

TPS6273x Programmable Output Voltage Ultra-Low Power Buck Converter

With Up to 50 mA / 200 mA Output Current

1 Features

- Industry's Highest Efficiency at Low Output Currents: > 90% With $I_{OUT} = 15 \mu\text{A}$
- Ultra-Low Power Buck Converter
 - TPS62736 Optimized for 50-mA Output Current
 - TPS62737 Optimized for 200-mA Output Current
 - 1.3-V to 5-V Resistor Programmable Output Voltage Range
 - 2-V to 5.5-V Input Operating Range
 - 380-nA and 375-nA Quiescent Current During Active Operation for TPS62736 and TPS62737
 - 10-nA Quiescent Current During Ship Mode Operation
 - 2% Voltage Regulation Accuracy
- 100% Duty Cycle (Pass Mode)
- EN1 and EN2 Control
 - Two Power-Off States:
 1. Shipmode (Full Power-Off State)
 2. Standby Mode Includes VIN_OK Indication
- Input Power-Good Indication (VIN_OK)
 - Push-Pull Driver
 - Resistor Programmable Threshold Level

2 Applications

- Ultra-Low Power Applications
- 2-Cell and 3-Cell Alkaline-Powered Applications
- Energy Harvesting
- Solar Chargers
- Thermal Electric Generator (TEG) Harvesting
- Wireless Sensor Networks (WSN)
- Low-Power Wireless Monitoring
- Environmental Monitoring
- Bridge and Structural Health Monitoring (SHM)
- Smart Building Controls
- Portable and Wearable Health Devices
- Entertainment System Remote Controls

3 Description

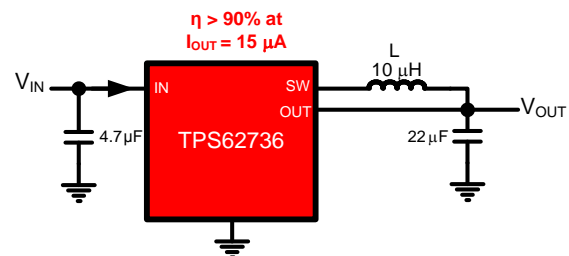
The TPS6273x family provides a highly integrated ultra low power buck converter solution that is well suited for meeting the special needs of ultra-low power applications such as energy harvesting. The TPS6273x provides the system with an externally programmable regulated supply to preserve the overall efficiency of the power-management stage compared to a linear step-down converter. This regulator is intended to step-down the voltage from an energy storage element such as a battery or super capacitor to supply the rail to low-voltage electronics. The regulated output has been optimized to provide high efficiency across low-output currents (<10 μA) to high currents (200 mA).

The TPS6273x integrates an optimized hysteretic controller for low-power applications. The internal circuitry uses a time-based sampling system to reduce the average quiescent current.

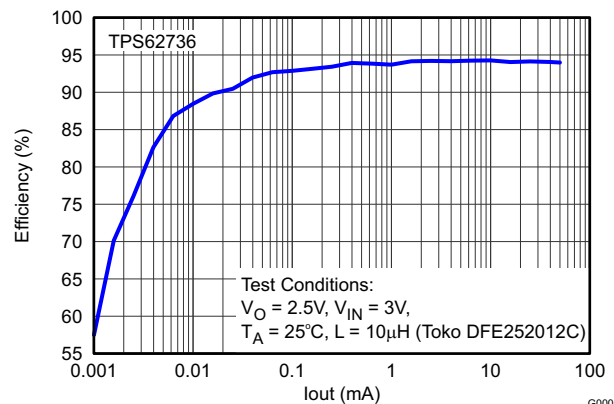
Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|-------------------|
| TPS6273x | VQFN (14) | 3.50 mm x 3.50 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Efficiency vs Output Current



6000



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4 Revision History

Changes from Revision B (July 2013) to Revision C

Page

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. **1**

Changes from Revision A (March 2013) to Revision B

Page

- Added the TPS62737 Pinout information
- Added graphs for TPS62737 to the Typical Characteristics.....
- Added the TPS62737 Application Circuit.
- Changed [Figure 72](#)
- Added [Figure 73](#)

Changes from Original (October 2012) to Revision A

Page

- Changed the device From: Preview To: Active

5 Description (continued)

To further assist users in the strict management of their energy budgets, the TPS6273x toggles the input power-good indicator to signal an attached microprocessor when the voltage on the input supply has dropped below a preset critical level. This signal is intended to trigger the reduction of load currents to prevent the system from entering an undervoltage condition. In addition, independent enable signals allow the system to control whether the converter is regulating the output, monitoring only the input voltage, or to shut down in an ultra-low quiescent sleep state.

The input power-good threshold and output regulator levels are programmed independently through external resistors.

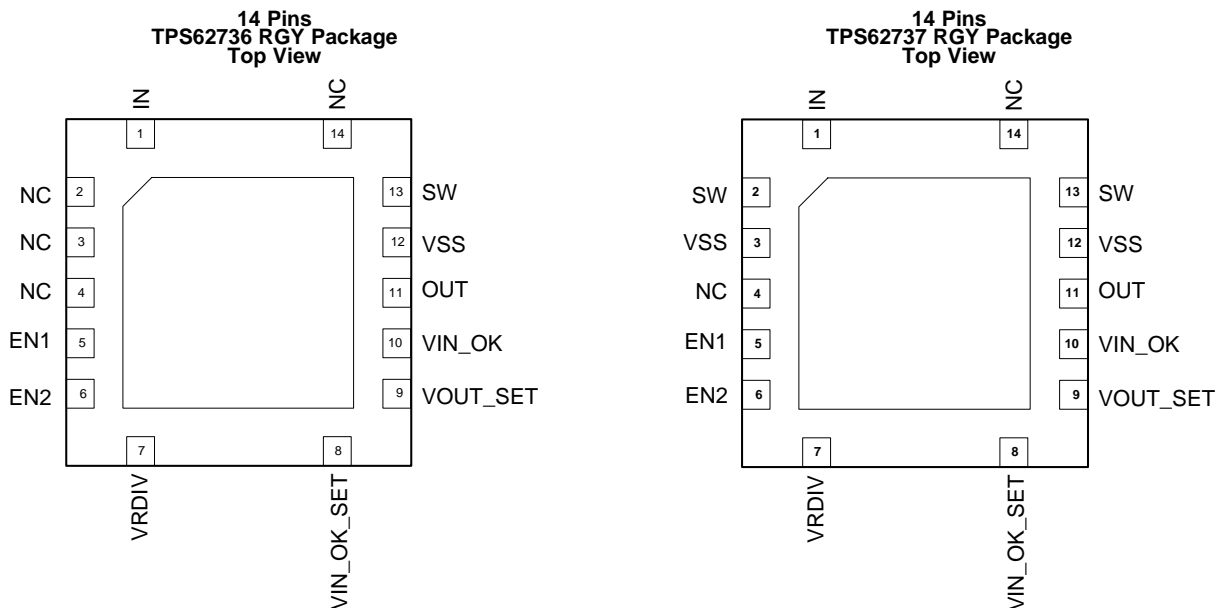
All the capabilities of TPS6273x are packed into a small footprint 14-lead 3.5-mm × 3.5-mm QFN package (RGY).

6 Device Voltage Options

| PART NO. | OUTPUT VOLTAGE | MAX OUTPUT CURRENT | INPUT UVLO |
|-------------------------|-----------------------|--------------------|------------|
| TPS62736 ⁽¹⁾ | Resistor Programmable | 50 mA | 2 V |
| TPS62737 ⁽¹⁾ | Resistor Programmable | 200 mA | 2 V |

(1) The RGY package is available in tape on reel. Add R suffix to order quantities of 3000 parts per reel, T suffix for 250 parts per reel.

7 Pin Configuration and Functions



Pin Functions

| NAME | PIN | | TYPE | DESCRIPTION |
|-------------|--------------|--------------|--------|--|
| | TPS62736 RGY | TPS62737 RGY | | |
| EN1 | 5 | 5 | Input | Digital input for chip enable, standby, and ship-mode. EN1 = 1 sets ship mode independent of EN2. EN1=0, EN2 = 0 disables the buck converter and sets standby mode. EN1=0, EN2=1 enables the buck converter. Do not leave either pin floating. |
| EN2 | 6 | 6 | Input | |
| IN | 1 | 1 | Input | Input supply to the buck regulator |
| NC | 2, 3, 4, 14 | 4, 14 | Input | Connect to VSS |
| OUT | 11 | 11 | Output | Step down (buck) regulator output |
| SW | 13 | 2, 13 | Input | Inductor connection to switching node |
| Thermal Pad | 15 | 15 | Input | Connect to VSS |
| VIN_OK | 10 | 10 | Output | Push-pull digital output for power-good indicator for the input voltage. Pulled up to VIN pin. |
| VIN_OK_SET | 8 | 8 | Input | Resistor divider input for VIN_OK threshold. Pull to VIN to disable. Do not leave pin floating. |
| VOUT_SET | 9 | 9 | Input | Resistor divider input for VOUT regulation level |
| VRDIV | 7 | 7 | Output | Resistor divider biasing voltage |
| VSS | 12 | 3, 12 | Input | Ground connection for the device |

8 Specifications

8.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|----------------|---|------|-----|------|
| Pin voltage | Input voltage range on IN, EN1, EN2, VRDIV, VIN_OK_SET, VOUT_SET, VIN_OK, OUT, SW, NC | -0.3 | 5.5 | V |
| TPS62736 | Peak currents | | 100 | mA |
| TPS62737 | Peak currents | | 370 | mA |
| T _J | Temperature range | -40 | 125 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to VSS/ground terminal

8.2 Handling Ratings

| | | MIN | MAX | UNIT | |
|--------------------|---------------------------|--|------|------|----|
| T _{stg} | Storage temperature range | -65 | 150 | °C | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | -1 | 1 | kV |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | -500 | 500 | V |
| | | Machine Model (MM) | -150 | 150 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|--|---|-----|-----|-----|------|
| IN | IN voltage range | 2 | | 5.5 | V |
| C _{IN} | TPS62736 Input Capacitance | 4.7 | | | μF |
| | TPS62737 Input Capacitance | 22 | | | |
| C _{OUT} | Output Capacitance | 10 | 22 | | μF |
| R ₁ + R ₂ + R ₃ | Total Resistance for setting reference voltage | | 13 | | MΩ |
| L _{BUCK} | TPS62736 Inductance | 4.7 | 10 | | μH |
| | TPS62737 Inductance | 10 | | | |
| T _A | TPS62736 Operating free air ambient temperature | -40 | | 85 | °C |
| | TPS62737 Operating free air ambient temperature | -20 | | 85 | |
| T _J | Operating junction temperature | -40 | | 105 | °C |

8.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPS6273x | UNIT |
|-------------------------------|--|----------|------|
| | | RGY | |
| | | 14 PINS | |
| θ _{JA} | Junction-to-ambient thermal resistance | 33.7 | °C/W |
| θ _{JCtop} | Junction-to-case (top) thermal resistance | 37.6 | |
| θ _{JB} | Junction-to-board thermal resistance | 10.1 | |
| ψ _{JT} | Junction-to-top characterization parameter | 0.4 | |
| ψ _{JB} | Junction-to-board characterization parameter | 10.3 | |
| θ _{JCbot} | Junction-to-case (bottom) thermal resistance | 2.9 | |

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report ([SPRA953](#)).

8.5 Electrical Characteristics

Over recommended ambient temperature range, typical values are at $T_A = 25^\circ\text{C}$. Unless otherwise noted, specifications apply for conditions of $V_{IN} = 4.2\text{ V}$, $V_{OUT} = 1.8\text{ V}$ External components, $C_{IN} = 4.7\text{ }\mu\text{F}$ for TPS62736 and $22\text{ }\mu\text{F}$ for TPS62737, $L_{BUCK} = 10\text{ }\mu\text{H}$, $C_{OUT} = 22\text{ }\mu\text{F}$.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---------------------------|---|--|--------------------------|------|----------------|---------------|----|
| QUIESCENT CURRENTS | | | | | | | |
| I_Q | TPS62736 Buck enabled state (EN1 = 0, EN2 = 1) | $V_{IN} = 2\text{ V}$, No load on V_{OUT} | | 380 | 550 | nA | |
| | TPS62736 Buck disabled VIN_OK active state (EN1 = 0, EN2 = 0) | | | 340 | 520 | | |
| | TPS62736 Ship mode state (EN1 = 1, EN2 = x) | | | 10 | 65 | | |
| | TPS62737 Buck enabled state (EN1 = 0, EN2 = 1) | | | | 375 | 600 | nA |
| | TPS62737 Buck disabled VIN_OK active state (EN1 = 0, EN2 = 0) | | | | 345 | 560 | |
| | TPS62737 Ship mode state (EN1 = 1, EN2 = x) | | | | 11 | 45 | |
| OUTPUT | | | | | | | |
| V_{BIAS} | Output regulation reference | | 1.205 | 1.21 | 1.217 | V | |
| V_{OUT} | TPS62736 Output regulation (<i>Spec does not include the resistor accuracy error</i>) | $I_{OUT} = 10\text{ mA}$; $1.3\text{ V} < V_{OUT} < 3.3\text{ V}$ | -2% | 0% | 2% | | |
| | TPS62737 Output regulation (<i>Spec does not include the resistor accuracy error</i>) | $I_{OUT} = 100\text{ mA}$; $1.3\text{ V} < V_{OUT} < 3.3\text{ V}$; | -2% | 0% | 2% | | |
| | TPS62736 Output line regulation | $I_{OUT} = 100\text{ }\mu\text{A}$; $V_{IN} = 2.4\text{ V to } 5.5\text{ V}$ | | 0.01 | | %/V | |
| | TPS62737 Output line regulation | $I_{OUT} = 10\text{ mA}$; $V_{IN} = 2.3\text{ V to } 5.5\text{ V}$ | | 0.31 | | | |
| | TPS62736 Output load regulation | $I_{OUT} = 100\text{ }\mu\text{A to } 50\text{ mA}$; $V_{IN} = 2.2\text{ V}$ | | 0.01 | | %/mA | |
| | TPS62737 Output load regulation | $I_{OUT} = 100\text{ }\mu\text{A to } 200\text{ mA}$; $V_{IN} = 2.2\text{ V}$; $-20^\circ\text{C} < T_A < 85^\circ\text{C}$ | | 0.01 | | %/mA | |
| | TPS62736 Output ripple | $V_{IN} = 4.2\text{ V}$, $I_{OUT} = 1\text{ mA}$; $C_{OUT} = 22\text{ }\mu\text{F}$ | | 20 | | mVpp | |
| | TPS62737 Output ripple | $V_{IN} = 4.2\text{ V}$, $I_{OUT} = 1\text{ mA}$; $C_{OUT} = 22\text{ }\mu\text{F}$ | | 40 | | mVpp | |
| | | Programmable voltage range for output voltage threshold | $I_{OUT} = 10\text{ mA}$ | 1.3 | $V_{IN} - 0.2$ | | V |
| V_{DO} | TPS62736 Drop-out-voltage when V_{IN} is less than $V_{OUT(SET)}$ | $V_{IN} = 2.1\text{ V}$, $V_{OUT(SET)} = 2.5\text{ V}$; $I_{OUT} = 10\text{ mA}$, 100% duty cycle | | 24 | 30 | mV | |
| | TPS62737 Drop-out-voltage when V_{IN} is less than $V_{OUT(SET)}$ | $V_{IN} = 2.1\text{ V}$, $V_{OUT(SET)} = 2.5\text{ V}$; $I_{OUT} = 100\text{ mA}$, 100% duty cycle | | 180 | 220 | mV | |
| $t_{START-STBY}$ | Startup time with EN1 low and EN2 transition to high (Standby Mode) | TPS62736, $C_{OUT} = 22\text{ }\mu\text{F}$ | | 400 | | μs | |
| | | TPS62737, $C_{OUT} = 22\text{ }\mu\text{F}$ | | 300 | | μs | |
| $t_{START-SHIP}$ | Startup time with EN2 high and EN1 transition from high to low (Ship Mode) | $C_{OUT} = 22\text{ }\mu\text{F}$ | | 100 | | ms | |

Electrical Characteristics (continued)

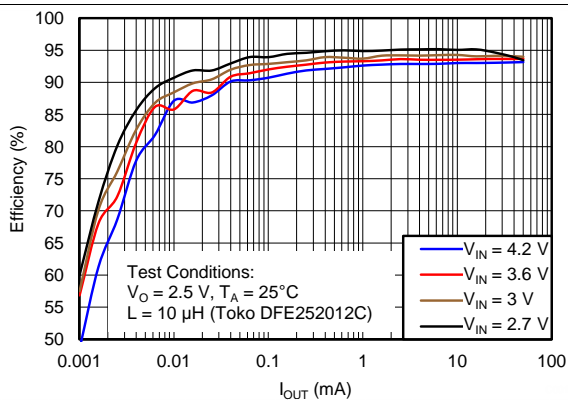
Over recommended ambient temperature range, typical values are at $T_A = 25^\circ\text{C}$. Unless otherwise noted, specifications apply for conditions of $V_{IN} = 4.2\text{ V}$, $V_{OUT} = 1.8\text{ V}$ External components, $C_{IN} = 4.7\text{ }\mu\text{F}$ for TPS62736 and $22\text{ }\mu\text{F}$ for TPS62737, $L_{BUCK} = 10\text{ }\mu\text{H}$, $C_{OUT} = 22\text{ }\mu\text{F}$.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|---|--|----------------|------|-----|----------|
| POWER SWITCH | | | | | | |
| $R_{DS(on)}$ | TPS62736 High-side switch ON resistance | $V_{IN} = 3\text{ V}$ | | 2.4 | 3 | Ω |
| | TPS62736 Low-side switch ON resistance | $V_{IN} = 3\text{ V}$ | | 1.1 | 1.5 | Ω |
| | TPS62737 High-side switch ON resistance | $V_{IN} = 2.1\text{ V}$ | | 1.8 | 2.2 | Ω |
| | TPS62737 Low-side switch ON resistance | $V_{IN} = 2.1\text{ V}$ | | 0.9 | 1.3 | Ω |
| I_{LIM} | TPS62736 Cycle-by-cycle current limit | $2.4\text{ V} < V_{IN} < 5.25\text{ V};$ $1.3\text{ V} < V_{OUT} < 3.3\text{ V}$ | 68 | 86 | 100 | mA |
| | TPS62737 Cycle-by-cycle current limit | $2.4\text{ V} < V_{IN} < 5.25\text{ V};$ $1.3\text{ V} < V_{OUT} < 3.3\text{ V};$ $-20^\circ\text{C} < T_A < 85^\circ\text{C}$ | 295 | 340 | 370 | mA |
| f_{SW} | Max switching frequency | | | 2 | | MHz |
| INPUT | | | | | | |
| $V_{IN-UVLO}$ | Input under voltage protection | V_{IN} falling | 1.91 | 1.95 | 2 | V |
| V_{IN-OK} | Input power-good programmable voltage range | | 2 | | 5.5 | V |
| $V_{IN-OK-ACC}$ | TPS62736 Accuracy of V_{IN-OK} setting | V_{IN} increasing | -2% | | 2% | |
| | TPS62737 Accuracy of V_{IN-OK} setting | | -3% | | 3% | |
| $V_{IN-OK-HYS}$ | Fixed hysteresis on V_{IN-OK} threshold, OK_HYST | V_{IN} increasing | | 40 | | mV |
| $V_{IN-OK-OH}$ | V_{IN-OK} output high threshold voltage | Load = $10\text{ }\mu\text{A}$ | $V_{IN} - 0.2$ | | | V |
| $V_{IN-OK-OL}$ | V_{IN-OK} output low threshold voltage | | | | 0.1 | V |
| EN1 and EN2 | | | | | | |
| V_{IH} | Voltage for EN High setting. Relative to V_{IN} | $V_{IN} = 4.2\text{ V}$ | $V_{IN} - 0.2$ | | | V |
| V_{IL} | Voltage for EN Low setting | | | | 0.2 | V |

8.6 Typical Characteristics

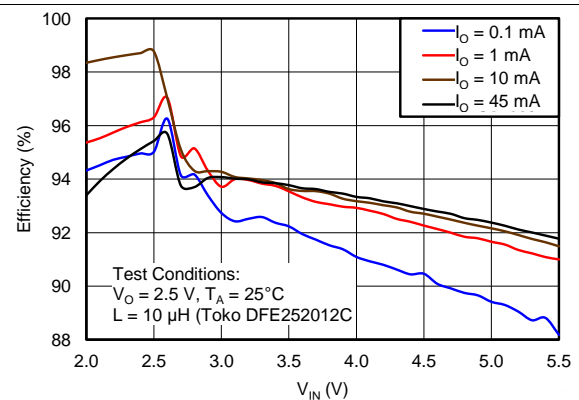
Table 1. Table of Graphs for TPS62736

| Unless otherwise noted, graphs were taken using Figure 62 with L = Toko 10 μ H DFE252012C | | | FIGURE |
|---|---------------------------------|-------------------|-----------|
| η | $V_O = 2.5$ V Efficiency | vs Output Current | Figure 1 |
| | | vs Input Voltage | Figure 2 |
| | $V_O = 1.8$ V Efficiency | vs Output Current | Figure 3 |
| | | vs Input Voltage | Figure 4 |
| | $V_O = 1.3$ V Efficiency | vs Output Current | Figure 5 |
| | | vs Input Voltage | Figure 6 |
| V_{OUT} (DC) | $V_O = 2.5$ V | vs Output Current | Figure 7 |
| | | vs Input Voltage | Figure 8 |
| | | vs Temperature | Figure 9 |
| | $V_O = 1.8$ V | vs Output Current | Figure 10 |
| | | vs Input Voltage | Figure 11 |
| | | vs Temperature | Figure 12 |
| | $V_O = 1.3$ V | vs Output Current | Figure 13 |
| | | vs Input Voltage | Figure 14 |
| | | vs Temperature | Figure 15 |
| I_{OUT} MAX (DC) | $V_O = 2.5$ V | vs Input Voltage | Figure 16 |
| | $V_O = 1.8$ V | | Figure 17 |
| | $V_O = 1.3$ V | | Figure 18 |
| Input IQ | EN1 = 1, EN2 = 0 (Ship Mode) | vs Input Voltage | Figure 19 |
| | EN1 = 0, EN2 = 0 (Standby Mode) | | Figure 20 |
| | EN1 = 0, EN2 = 1 (Active Mode) | | Figure 21 |
| Switching Frequency | $V_O = 2.5$ V | vs Output Current | Figure 23 |
| | | vs Input Voltage | Figure 24 |
| Output Ripple | $V_O = 2.5$ V | vs Output Current | Figure 25 |
| | | vs Input Voltage | Figure 26 |



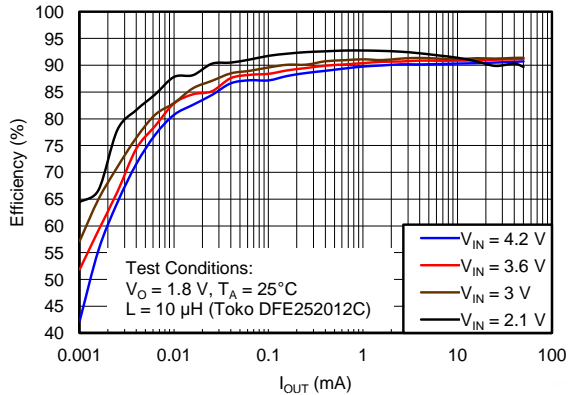
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 1. Efficiency vs Output Current, $V_{OUT} = 2.5$ V



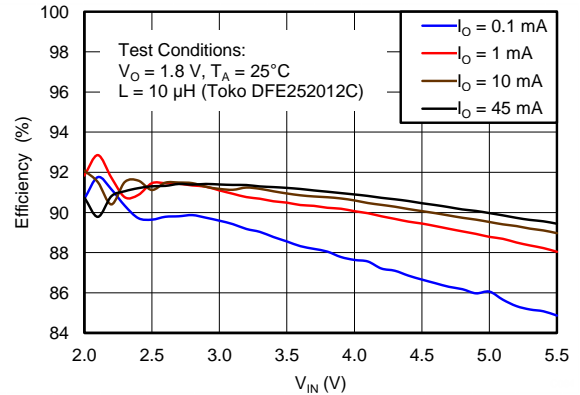
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 2. Efficiency vs Input Voltage, $V_{OUT} = 2.5$ V



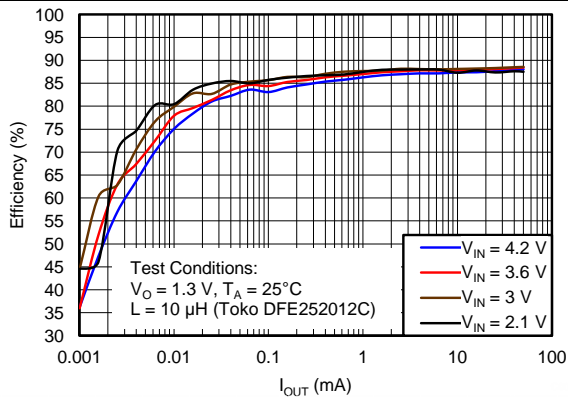
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 3. Efficiency vs Output Current, $V_{OUT} = 1.8\text{ V}$



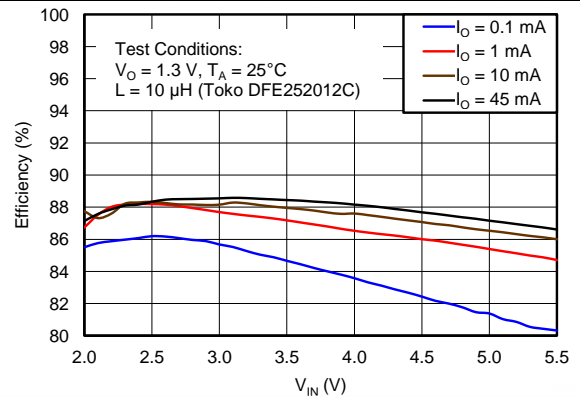
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 4. Efficiency vs Input Voltage, $V_{OUT} = 1.8\text{ V}$



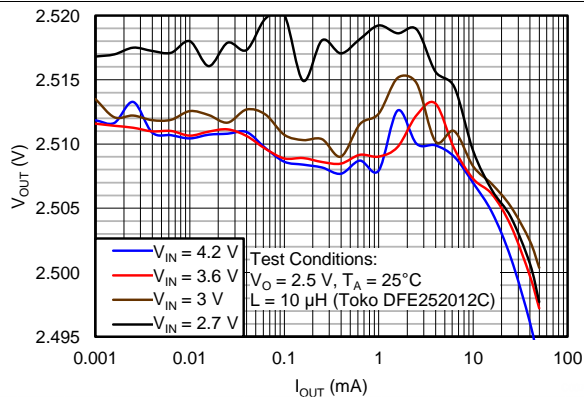
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 5. Efficiency vs Output Current, $V_{OUT} = 1.3\text{ V}$



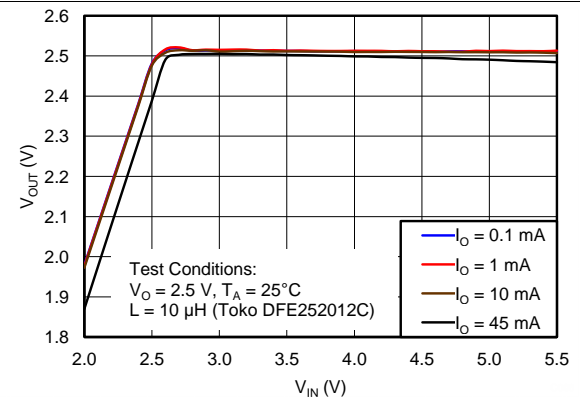
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 6. Efficiency vs Input Voltage, $V_{OUT} = 1.3\text{ V}$



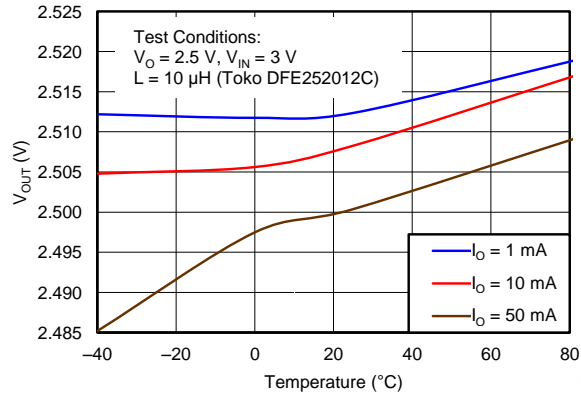
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 7. Output Voltage vs Output Current, $V_{OUT} = 2.5\text{ V}$



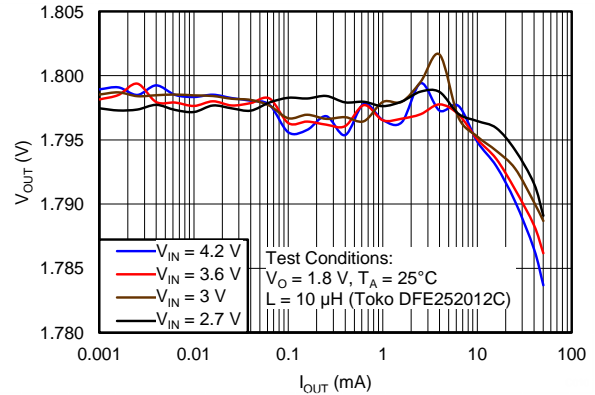
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 8. Output Voltage vs Input Voltage, $V_{OUT} = 2.5\text{ V}$



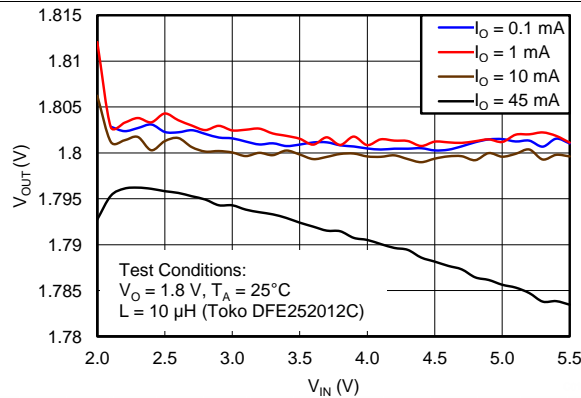
IN = Sourceter configured as voltage source and measuring current
 OUT = sourceter configured as current source to sink current and VCOMP > VOUT
 Thermal stream provided temperature variation

Figure 9. Output Voltage vs Temperature, $V_{OUT} = 2.5\text{ V}$



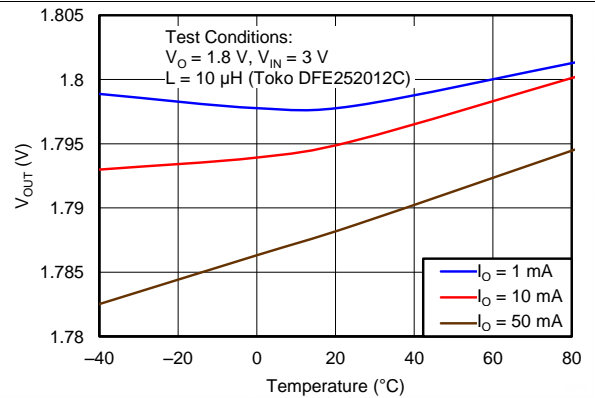
IN = Sourceter configured as voltage source and measuring current
 OUT = sourceter configured as current source to sink current and VCOMP > VOUT

Figure 10. Output Voltage vs Output Current, $V_{OUT} = 1.8\text{ V}$



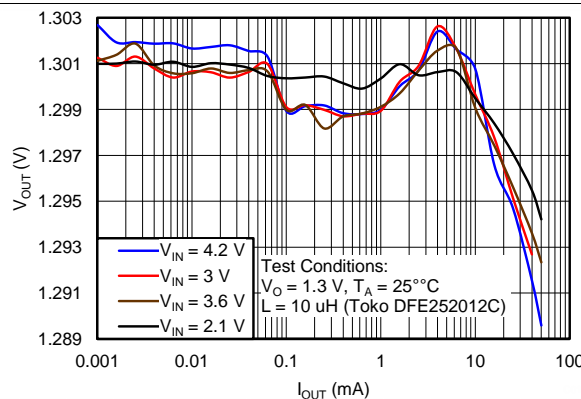
IN = Sourceter configured as voltage source and measuring current
 OUT = sourceter configured as current source to sink current and VCOMP > VOUT

Figure 11. Output Voltage vs Input Voltage, $V_{OUT} = 1.8\text{ V}$



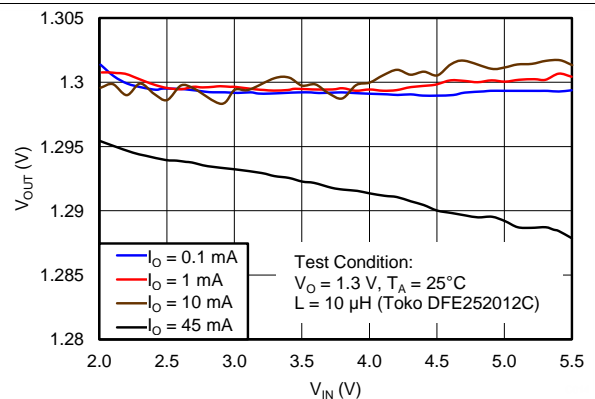
IN = Sourceter configured as voltage source and measuring current
 OUT = sourceter configured as current source to sink current and VCOMP > VOUT
 Thermal stream provided temperature variation

Figure 12. Output Voltage vs Temperature, $V_{OUT} = 1.8\text{ V}$



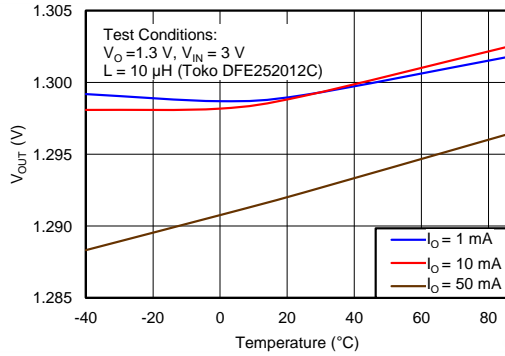
IN = Sourceter configured as voltage source and measuring current
 OUT = sourceter configured as current source to sink current and VCOMP > VOUT

Figure 13. Output Voltage vs Output Current, $V_{OUT} = 1.3\text{ V}$



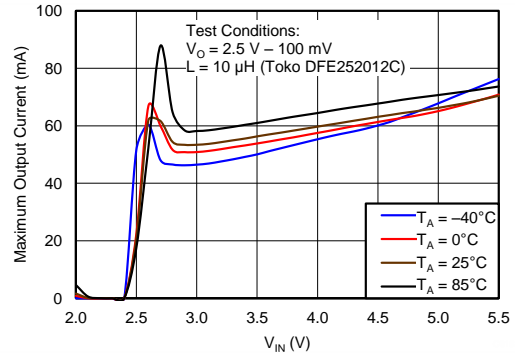
IN = Sourceter configured as voltage source and measuring current
 OUT = sourceter configured as current source to sink current and VCOMP > VOUT

Figure 14. Output Voltage vs Input Voltage, $V_{OUT} = 1.3\text{ V}$



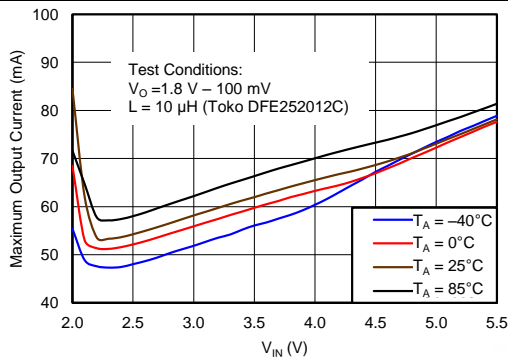
IN = Sourcemeter configured as voltage source and measuring current
 VOUT = sourcemeter configured as current source to sink current and VCOMP > VOUT
 Thermal stream provided temperature variation

Figure 15. Output Voltage vs Temperature, $V_{OUT} = 1.3\text{ V}$



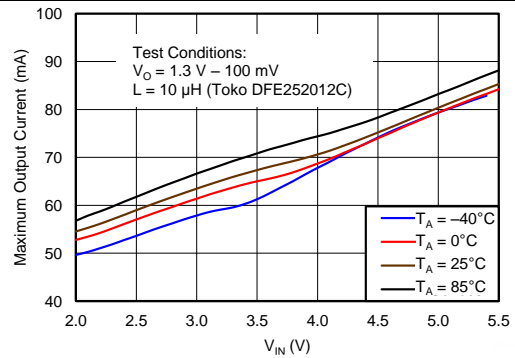
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to increasingly sink current until $V(OUT) < V_{OUT} - 100\text{ mV}$
 Thermal stream provided temperature variation

Figure 16. Maximum Output Current vs Input Voltage, $V_{OUT} = 2.5\text{ V}$



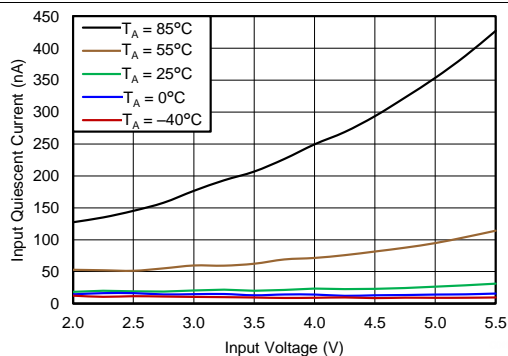
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to increasingly sink current until $V(OUT) < V_{OUT} - 100\text{ mV}$
 Thermal stream provided temperature variation

Figure 17. Maximum Output Current vs Input Voltage, $V_{OUT} = 1.8\text{ V}$



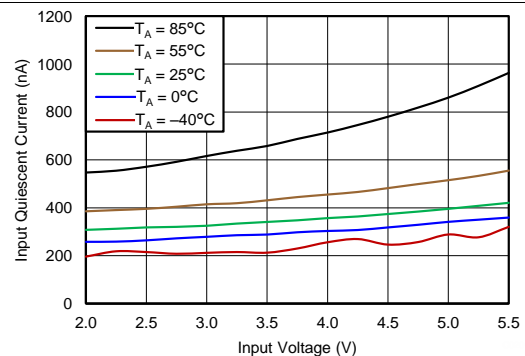
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to increasingly sink current until $V(OUT) < V_{OUT} - 100\text{ mV}$
 Thermal stream provided temperature variation

Figure 18. Maximum Output Current vs Input Voltage, $V_{OUT} = 1.3\text{ V}$



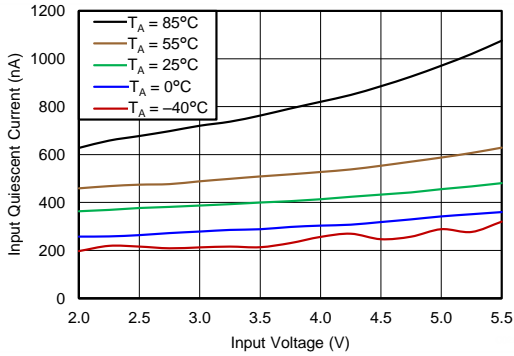
IN = Sourcemeter configured as voltage source and measuring current
 OUT = open; EN1 = high; EN2 = x
 Thermal stream provided temperature variation

Figure 19. Input Quiescent Current vs Input Voltage Ship Mode



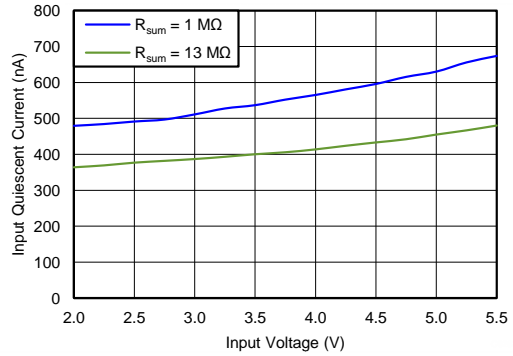
IN = Sourcemeter configured as voltage source and measuring current
 OUT = open; EN1 = EN2 = low
 Thermal stream provided temperature variation

Figure 20. Input Quiescent Current vs Input Voltage Standby Mode



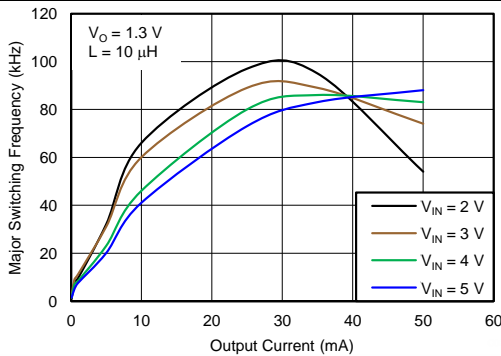
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as voltage source > VOUT to prevent switching
 Thermal stream provided temperature variation

Figure 21. Input Quiescent Current vs Input Voltage Active Mode



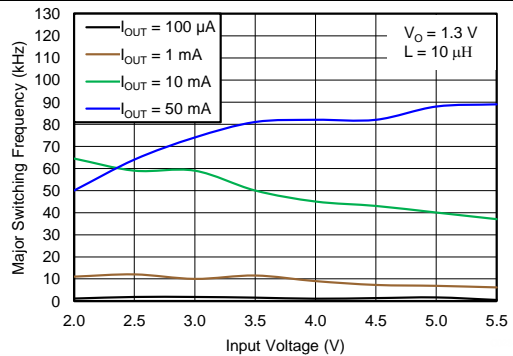
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as voltage source > VOUT to prevent switching
 Thermal stream provided temperature variation

Figure 22. Input Quiescent Current vs Input Voltage Active Mode where $R_{SUM} = R1 + R2 + R3$



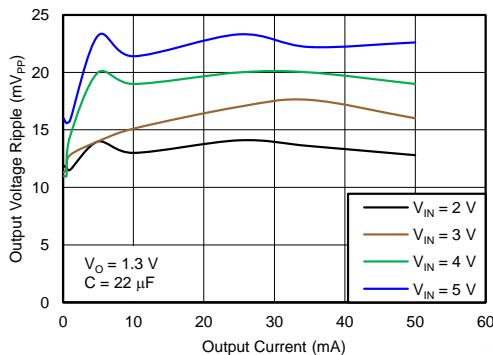
IN = Sourcemeter configured as voltage source
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 23. Major Switching Frequency vs Output Current



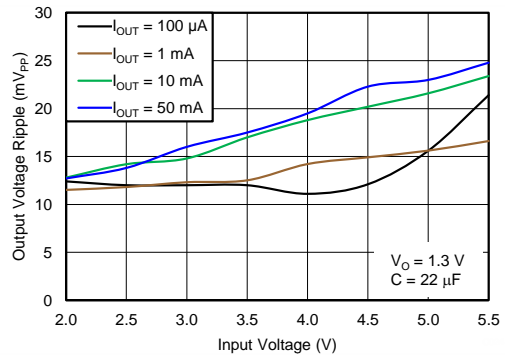
IN = Sourcemeter configured as voltage source
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 24. Major Switching Frequency vs Input Voltage



IN = Sourcemeter configured as voltage source
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT
 Scope probe with small ground lead used to measure ripple across COUT

Figure 25. Output Voltage Ripple vs Output Current

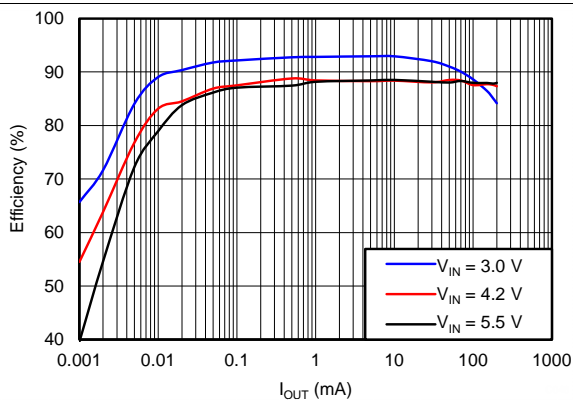


IN = Sourcemeter configured as voltage source
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT
 Scope probe with small ground lead used to measure ripple across COUT

Figure 26. Output Voltage Ripple vs Input Voltage

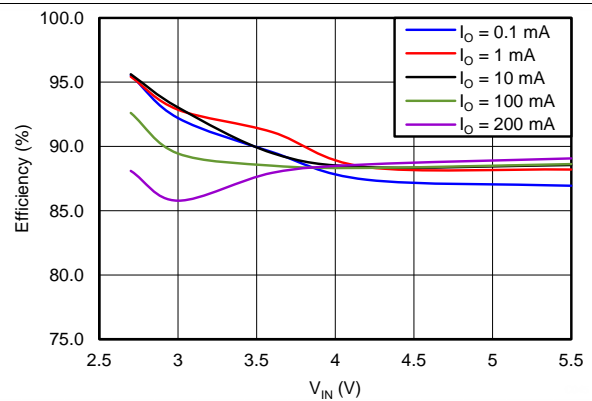
Table 2. Table of Graphs for TPS62737

| Unless otherwise noted, graphs were taken using Figure 52 with L = Toko 10 µH DFE252012C | | | FIGURE |
|--|---------------------------------|-------------------|-----------|
| η | $V_O = 2.5\text{ V}$ Efficiency | vs Output Current | Figure 27 |
| | | vs Input Voltage | Figure 28 |
| | $V_O = 1.8\text{ V}$ Efficiency | vs Output Current | Figure 29 |
| | | vs Input Voltage | Figure 30 |
| | $V_O = 1.3\text{ V}$ Efficiency | vs Output Current | Figure 31 |
| | | vs Input Voltage | Figure 32 |
| V_{OUT} (DC) | $V_O = 2.5\text{ V}$ | vs Output Current | Figure 33 |
| | | vs Input Voltage | Figure 33 |
| | | vs Temperature | Figure 35 |
| | $V_O = 1.8\text{ V}$ | vs Output Current | Figure 36 |
| | | vs Input Voltage | Figure 37 |
| | | vs Temperature | Figure 38 |
| | $V_O = 1.3\text{ V}$ | vs Output Current | Figure 39 |
| | | vs Input Voltage | Figure 40 |
| | | vs Temperature | Figure 41 |
| $I_{OUT\ MAX}$ (DC) | $V_O = 2.5\text{ V}$ | vs Input Voltage | Figure 42 |
| | $V_O = 1.8\text{ V}$ | | Figure 43 |
| | $V_O = 1.3\text{ V}$ | | Figure 44 |
| Input IQ | EN1 = 1, EN2 = 0 (Ship Mode) | vs Input Voltage | Figure 45 |
| | EN1 = 0, EN2 = 0 (Standby Mode) | | Figure 46 |
| | EN1 = 0, EN2 = 1 (Active Mode) | | Figure 47 |
| Switching Frequency | $V_O = 1.8\text{ V}$ | vs Output Current | Figure 48 |
| | | vs Input Voltage | Figure 49 |
| Output Ripple | $V_O = 1.8\text{ V}$ | vs Output Current | Figure 51 |
| | | vs Input Voltage | Figure 51 |



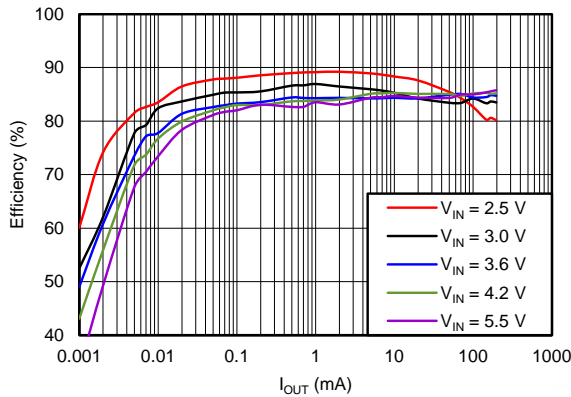
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 27. Efficiency vs Output Current, $V_{OUT} = 2.5\text{ V}$



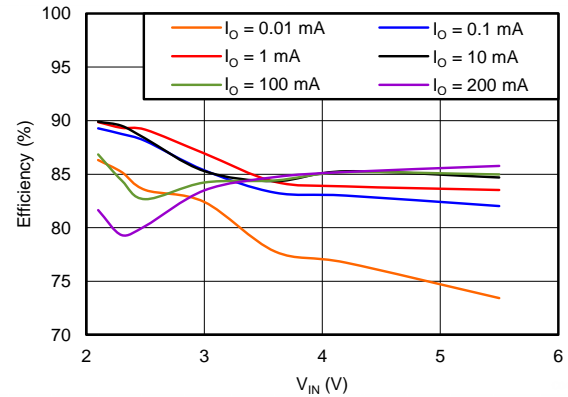
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 28. Efficiency vs Input Voltage, $V_{OUT} = 2.5\text{ V}$



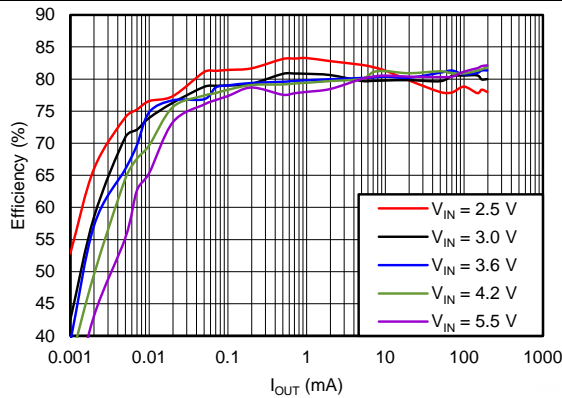
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 29. Efficiency vs Output Current, $V_{OUT} = 1.8\text{ V}$



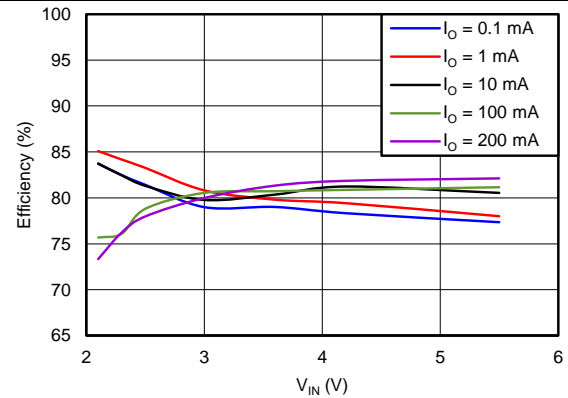
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 30. Efficiency vs Input Voltage, $V_{OUT} = 1.8\text{ V}$



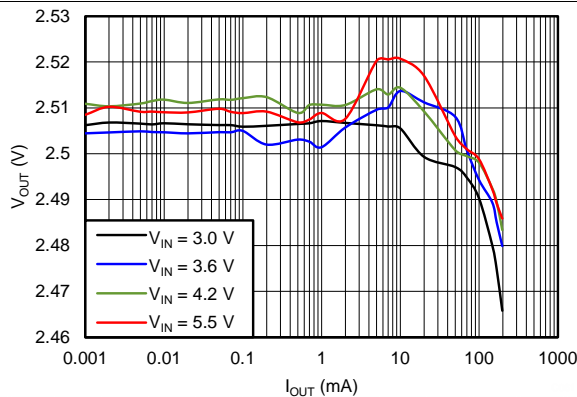
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 31. Efficiency vs Output Current, $V_{OUT} = 1.3\text{ V}$



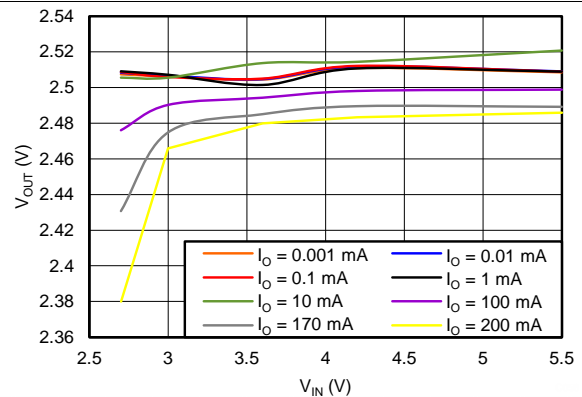
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 32. Efficiency vs Input Voltage, $V_{OUT} = 1.3\text{ V}$



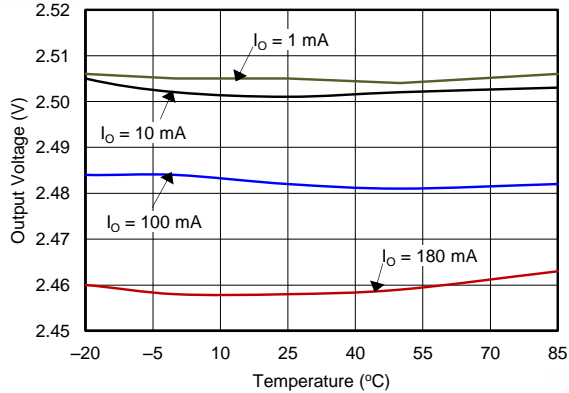
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 33. Output Voltage vs Output Current, $V_{OUT} = 2.5\text{ V}$



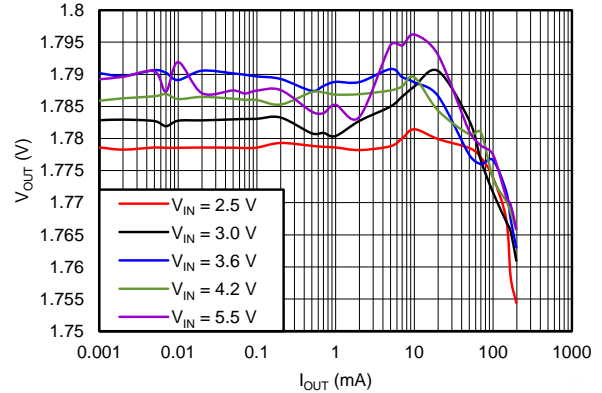
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 34. Output Voltage vs Input Voltage, $V_{OUT} = 2.5\text{ V}$



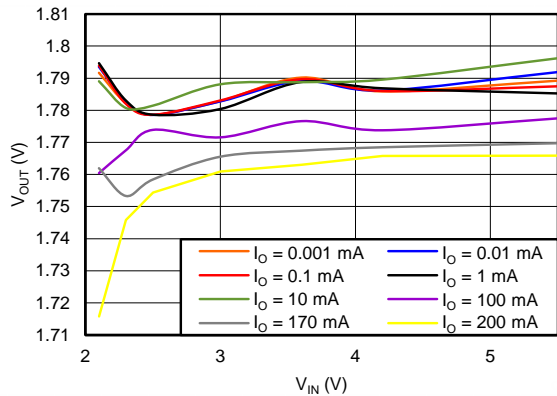
IN = Sourceter configured as voltage source and measuring current
 OUT = sourceter configured as current source to sink current and VCOMP > VOUT
 Thermal stream provided temperature variation

Figure 35. Output Voltage vs Temperature, $V_{OUT} = 2.5\text{ V}$



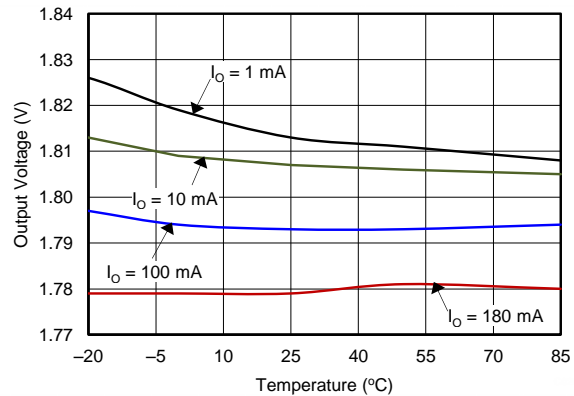
IN = Sourceter configured as voltage source and measuring current
 OUT = sourceter configured as current source to sink current and VCOMP > VOUT

Figure 36. Output Voltage vs Output Current, $V_{OUT} = 1.8\text{ V}$



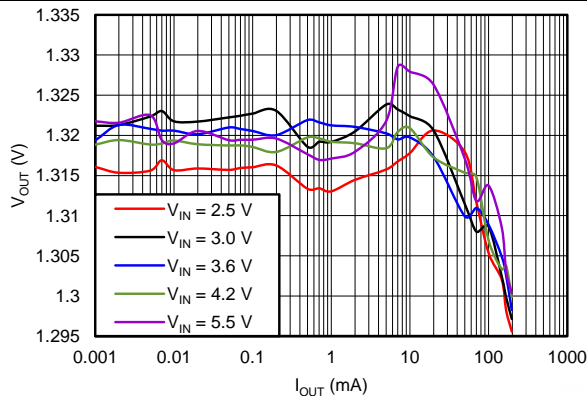
IN = Sourceter configured as voltage source and measuring current
 OUT = sourceter configured as current source to sink current and VCOMP > VOUT

Figure 37. Output Voltage vs Input Voltage, $V_{OUT} = 1.8\text{ V}$



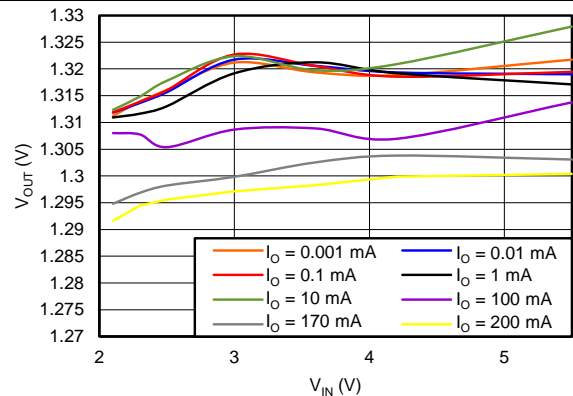
IN = Sourceter configured as voltage source and measuring current
 OUT = sourceter configured as current source to sink current and VCOMP > VOUT
 Thermal stream provided temperature variation

Figure 38. Output Voltage vs Temperature, $V_{OUT} = 1.8\text{ V}$



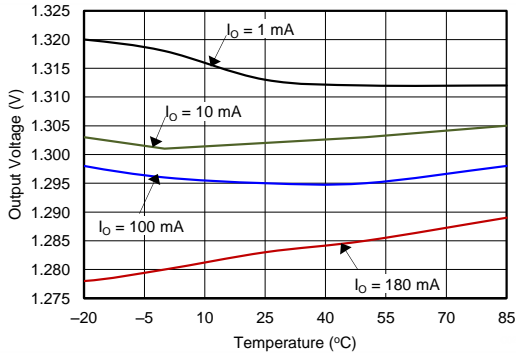
IN = Sourceter configured as voltage source and measuring current
 OUT = sourceter configured as current source to sink current and VCOMP > VOUT

Figure 39. Output Voltage vs Output Current, $V_{OUT} = 1.3\text{ V}$



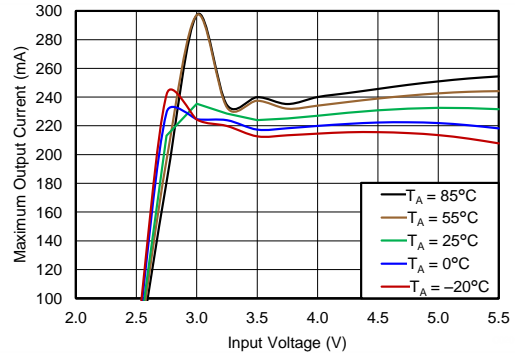
IN = Sourceter configured as voltage source and measuring current
 OUT = sourceter configured as current source to sink current and VCOMP > VOUT

Figure 40. Output Voltage vs Input Voltage, $V_{OUT} = 1.3\text{ V}$



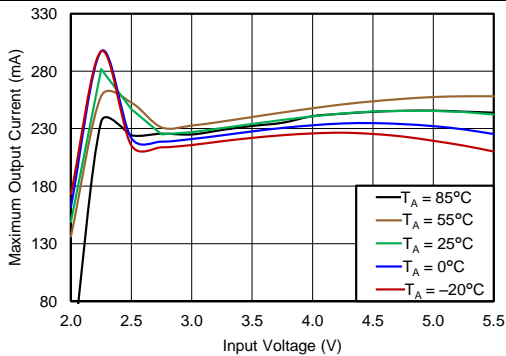
IN = Sourceter configured as voltage source and measuring current
 OUT = sourceter configured as current source to sink current and VCOMP > VOUT
 Thermal stream provided temperature variation

Figure 41. Output Voltage vs Temperature, $V_{OUT} = 1.3 \text{ V}$



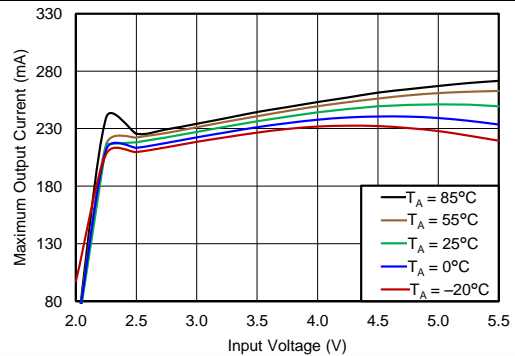
IN = Sourceter configured as voltage source and measuring current
 OUT = sourceter configured as current source to increasingly sink current until $V(OUT) < V_{OUT} - 100 \text{ mV}$
 Thermal stream provided temperature variation

Figure 42. Maximum Output Current vs Input Voltage $V_{OUT} = 2.5 \text{ V}$



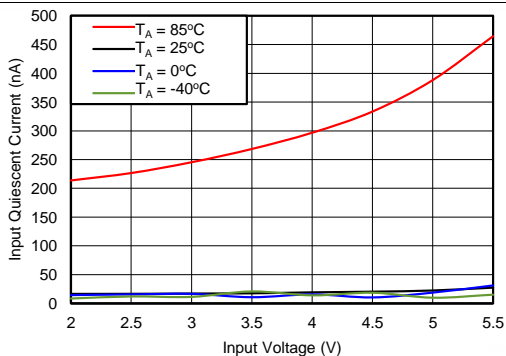
IN = Sourceter configured as voltage source and measuring current
 OUT = sourceter configured as current source to increasingly sink current until $V(OUT) < V_{OUT} - 100 \text{ mV}$
 Thermal stream provided temperature variation

Figure 43. Maximum Output Current vs Input Voltage, $V_{OUT} = 1.8 \text{ V}$



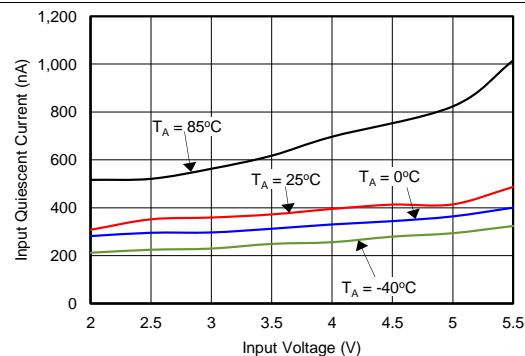
IN = Sourceter configured as voltage source and measuring current
 OUT = sourceter configured as current source to increasingly sink current until $V(OUT) < V_{OUT} - 100 \text{ mV}$
 Thermal stream provided temperature variation

Figure 44. Maximum Output Current vs Input Voltage, $V_{OUT} = 1.3 \text{ V}$



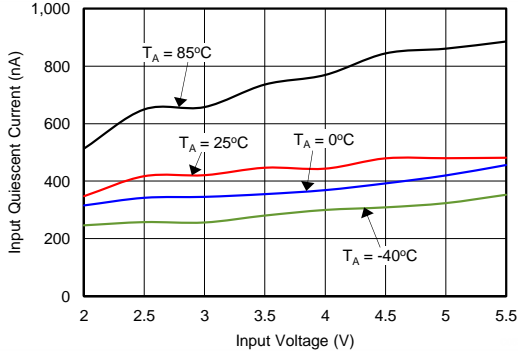
IN = Sourceter configured as voltage source and measuring current
 OUT = open; EN1 = high; EN2 = x
 Thermal stream provided temperature variation

Figure 45. Input Quiescent Current vs Input Voltage Ship Mode



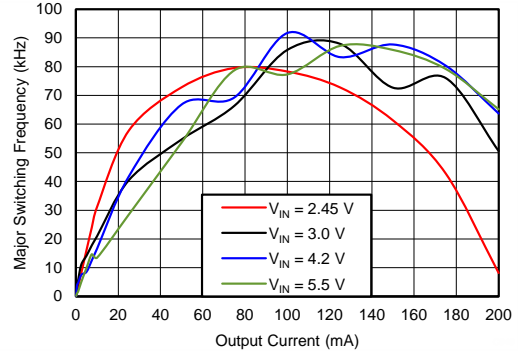
IN = Sourceter configured as voltage source and measuring current
 OUT = open; EN1 = EN2 = low
 Thermal stream provided temperature variation

Figure 46. Input Quiescent Current vs Input Voltage Standby Mode



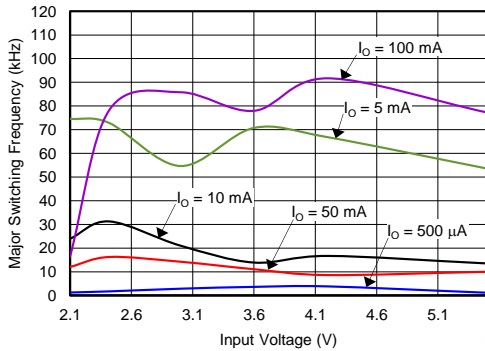
IN = Sourcemeter configured as voltage source and measuring current
 OUT = sourcemeter configured as voltage source > VOUT to prevent switching
 Thermal stream provided temperature variation

Figure 47. Input Quiescent Current vs Input Voltage Active Mode



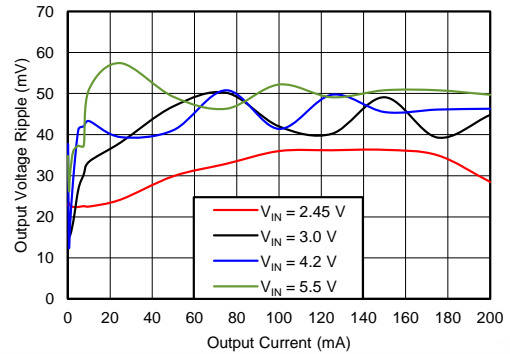
IN = Sourcemeter configured as voltage source
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 48. Major Switching Frequency vs Output Current



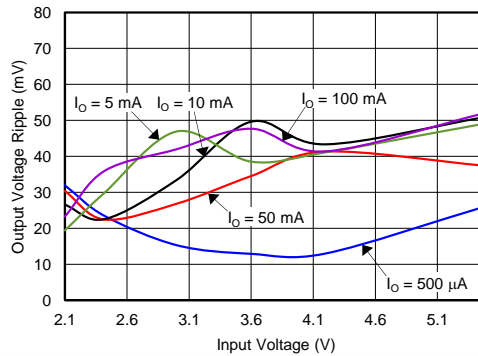
IN = Sourcemeter configured as voltage source
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT

Figure 49. Major Switching Frequency vs Input Voltage



IN = Sourcemeter configured as voltage source
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT
 Scope probe with small ground lead used to measure ripple across COUT

Figure 50. Output Voltage Ripple vs Output Current



IN = Sourcemeter configured as voltage source
 OUT = sourcemeter configured as current source to sink current and VCOMP > VOUT
 Scope probe with small ground lead used to measure ripple across COUT

Figure 51. Output Voltage Ripple vs Input Voltage

Feature Description (continued)

the voltage on VIN reaches the UVLO condition. The UVLO level is continuously monitored. The buck regulator continues to operate in pass (100% duty cycle) mode, passing the input voltage to the output, as long as VIN is greater than UVLO and less than VIN minus I_{OUT} times R_{DS(on)} of the high-side FET (that is, VIN – I_{OUT} × R_{DS(on)-HS}). In order to save power from being dissipated through other ICs on this supply rail while allowing for a faster wake up time, the buck regulator can be enabled and disabled through the EN2 pin for systems that desire to completely turn off the regulated output.

9.3.2 Programming OUT Regulation Voltage and VIN_OK

To set the proper output-regulation voltage and input voltage power-good comparator, the external resistors must be carefully selected. [Figure 62](#) illustrates an application diagram which uses the minimal resistor count for setting both VOUT and VIN_OK. Note that VBIAS is nominally 1.21 V per the electrical specification table. Referring to [Figure 52](#), the OUT DC set point is given by [Equation 1](#).

$$V_{OUT} = V_{BIAS} \left(\frac{R_1 + R_2 + R_3}{R_1 + R_2} \right) \quad (1)$$

The VIN_OK setting is given by [Equation 2](#).

$$VIN_OK = V_{BIAS} \left(\frac{R_1 + R_2 + R_3}{R_1} \right) \quad (2)$$

The sum of the resistors is recommended to be no greater than 13 MΩ, that is, R_{SUM} = R₁ + R₂ + R₃ = 13 MΩ. Due to the sampling operation of the output resistors, lowering R_{SUM} only increases quiescent current slightly as can be seen in [Figure 22](#). Higher resistors may result in poor output voltage regulation and/or input voltage power-good threshold accuracies due to noise pickup through the high-impedance pins or reduction of effective resistance due to parasitic resistance created from board assembly residue. See [Layout](#) for more details.

If it is preferred to separate the VOUT and VIN_OK resistor strings, two separate strings of resistors could be used as shown in [Figure 62](#). The OUT DC set point is then given by [Equation 3](#).

$$V_{OUT} = V_{BIAS} \left(\frac{R_3 + R_4}{R_4} \right) \quad (3)$$

The VIN_OK setting is then given by [Equation 4](#).

$$VIN_OK = V_{BIAS} \left(\frac{R_1 + R_2}{R_1} \right) \quad (4)$$

If it is preferred to disable the VIN_OK setting, the VIN_OK_SET pin can be tied to VIN. To set VOUT in this configuration, use [Equation 3](#). To tighten the DC set point accuracy, use external resistors with better than 1% resistor tolerance. Because output voltage ripple has a large effect on input line regulation and the output load regulation, using a larger output capacitor will improve both line and load regulation.

9.3.3 Nano-Power Management and Efficiency

The high efficiency of the TPS6273x is achieved through the proprietary Nano-Power management circuitry and algorithm. This feature essentially samples and holds all references in order to reduce the average quiescent current. That is, the internal circuitry is only active for a short period of time and then off for the remaining period of time at the lowest feasible duty cycle. A portion of this feature can be observed in [Figure 66](#) where the VRDIV node is monitored. Here, the VRDIV node provides a connection to the input (larger voltage level) and generates the output reference (lower-voltage level) for a short period of time. The divided down value of input voltage is compared to VBIAS and the output voltage reference is sampled and held to get the VOUT_SET point. Because this biases a resistor string, the current through these resistors is only active when the Nano-Power management circuitry makes the connection — hence, reducing the overall quiescent current due to the resistors. This process repeats every 64 ms. Similarly, the VIN_OK level is monitored every 64 ms, as shown in [Figure 55](#).

Feature Description (continued)

The efficiency versus output current and efficiency versus input voltage are plotted for three different output voltages for both the TPS62736 and TPS62737 devices in [Typical Characteristics](#). All data points were captured by averaging the overall input current. This must be done, due to the periodic biasing scheme implemented through the Nano-Power management circuitry. The input current efficiency data was gathered using a source meter set to average over at least 25 samples and at the highest accuracy sampling rate. Each data point takes a long period of time to gather in order to properly measure the resulting input current when calculating the efficiency.

9.4 Device Functional Modes

9.4.1 Enable Controls

There are two enable pins implemented in the TPS6273x in order to maximize the flexibility of control for the system. The EN1 pin is considered to be the chip enable. If EN1 is set to a 1 then the entire chip is placed into ship mode. If EN1 is 0 then the chip is enabled. EN2 enables and disables the switching of the buck converter. When EN2 is low, the internal circuitry remains ON and the VIN_OK indicator still functions. This can be used to disable down-stream electronics in case of a low input-supply condition. When EN2 is 1, the buck converter operates normally.

Table 3. Enable Functionality Table

| EN1 PIN | EN2 PIN | FUNCTIONAL STATE |
|---------|---------|--|
| 0 | 0 | Partial standby mode. Buck switching converter is off, but VIN_OK indication is on |
| 0 | 1 | Buck mode and VIN_OK enabled |
| 1 | x | Full standby mode. Switching converter and VIN_OK indication is off (ship mode) |

9.4.2 Startup Behavior

The TPS6273x has two startup responses: 1) from the ship-mode state (EN1 transitions from high to low), and 2) from the standby state (EN2 transitions from low to high). The first startup response out of the ship-mode state has the longest time duration due to the internal circuitry being disabled. This response is shown in [Figure 70](#) for the TPS62736 and [Figure 60](#) for the TPS62737. The startup time takes approximately 100 ms due to the internal Nano-Power management circuitry needing to complete the 64 ms sample and hold cycle.

Startup from the standby state is shown in [Figure 71](#) for the TPS62736 and [Figure 61](#) for the TPS62737. This response is much faster due to the internal circuitry being pre-enabled. The startup time from this state is entirely dependent on the size of the output capacitor. The larger the capacitor, the longer it will take to charge during startup. The TPS6273x can startup into a prebiased output voltage.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS62736/7 are step down DC-DC converters. Their low quiescent currents make them ideal for battery powered systems that are operated at low duty cycles in order to achieve low total power levels.

10.2 Typical Applications

10.2.1 TPS62737 3-Resistor Typical Application Circuit

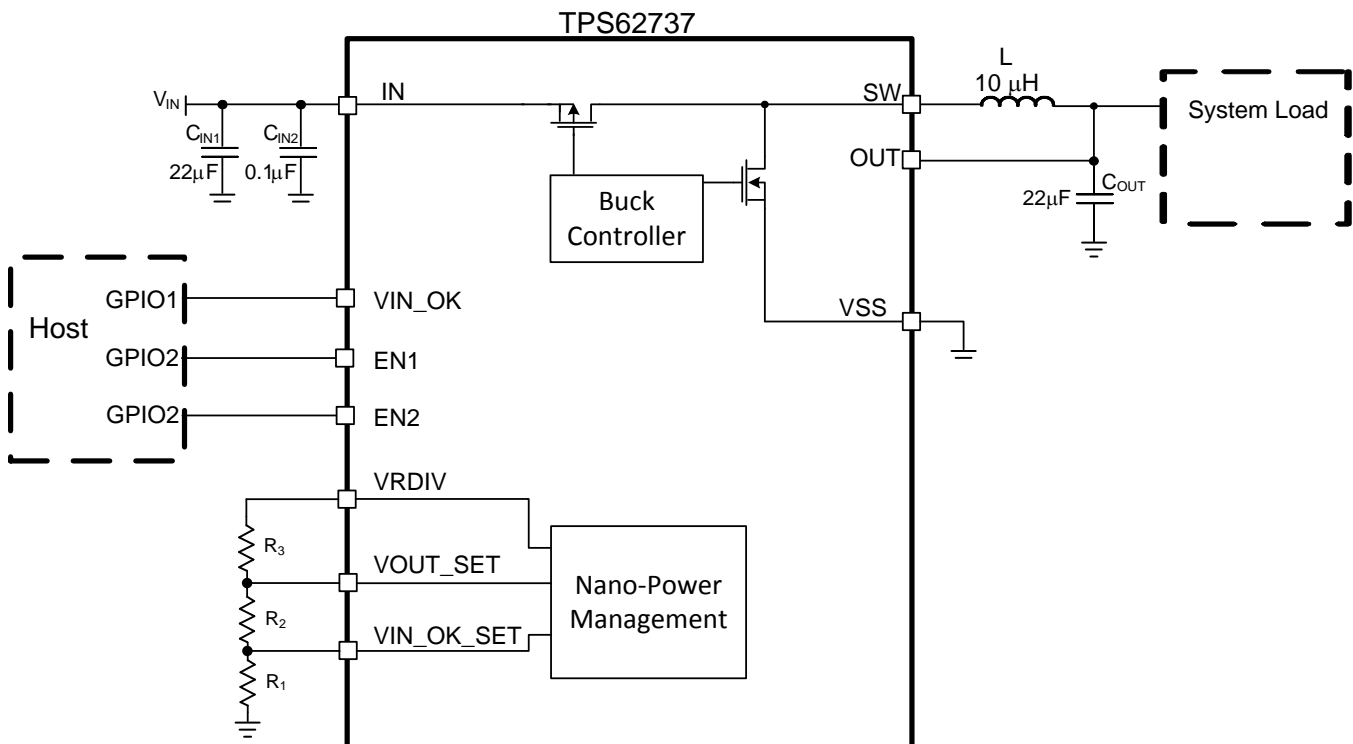


Figure 52. TPS62737 3-Resistor Typical Application Circuit

10.2.1.1 Design Requirements

A 1.8-V, up to 200 mA regulated power rail is needed. The VIN_OK comparator should indicate when the input voltage drops below 2.9 V. No large load transients are expected.

10.2.1.2 Detailed Design Procedure

The recommended 10-µH inductor (TOKO DFE252012C) and 22-µF input capacitor are used. Since no large load transients are expected, the minimum 22-µF output capacitor is used. Had a large load transient been expected, we would have sized the capacitor using $ITRAN = C_{OUT} \times \Delta V_{OUT} / \Delta TIME$ where ΔV_{OUT} is amount of VOUT droop allowed for the time of the transient.

First set $RSUM = R1 + R2 + R3 = 13 \text{ M}\Omega$ then solve Equation 2 for $R1 = V_{BIAS} \times RSUM / VIN_OK = 1.21 \text{ V} \times 13 \text{ M}\Omega / 2.9 \text{ V} = 5.42 \text{ M}\Omega \rightarrow 5.49 \text{ M}\Omega$ as the closest 1 % resistor.

Typical Applications (continued)

Then solve [Equation 2](#) for $R2 = V_{BIAS} \times R_{SUM} / V_{OUT} - R1 = 1.21 \text{ V} \times 13 \text{ M}\Omega / 1.8 \text{ V} - 5.42 \text{ M}\Omega = 3.32 \text{ M}\Omega \rightarrow 3.4 \text{ M}\Omega$ as the closest 1% resistor.

Finally $R3 = R_{SUM} - R1 - R2 = 13 \text{ M}\Omega - 5.42 \text{ M}\Omega - 3.32 \text{ M}\Omega = 4.26 \text{ M}\Omega \rightarrow 4.32 \text{ M}\Omega$ as the closest 1% resistor.

These values yield $V_{OUT} = 1.79 \text{ V}$ and V_{IN_OK} threshold = 2.91 V.

If using 4 resistors, see [Resistor Selection](#) for guidance on sizing the resistors.

10.2.1.2.1 Inductor Selection

The internal-control circuitry is designed to control the switching behavior with a nominal inductance of $10 \mu\text{H} \pm 20\%$. The saturation current of the inductor should be at least 25% higher than the maximum cycle-by-cycle current limit per the electrical specs table (I_{LIM}) in order to account for load transients. Because this device is a hysteretic controller, it is a naturally stable system (single order transfer function). However, the smaller the inductor value is, the faster the switching currents are. The speed of the peak current detect circuit sets the inductor of the TPS62736 lower bound to $4.7 \mu\text{H}$. When using a $4.7 \mu\text{H}$, the peak inductor current will increase when compared to that of a $10\text{-}\mu\text{H}$ inductor. The steady-state operation with a $4.7\text{-}\mu\text{H}$ inductor with a 50-mA load for the TPS62736 is shown in [Figure 65](#).

A list of inductors recommended for this device is shown in [Table 4](#).

Table 4. Recommended Inductors

| INDUCTANCE (μH) | DIMENSIONS (mm) | PART NUMBER | MANUFACTURER |
|------------------------------|-----------------|-------------------|--------------|
| 10 | 2.0 x 2.5 x 1.2 | DFE252012C-H-100M | Toko |
| 10 | 4.0 x 4.0 x 1.7 | LPS4018-103M | Coilcraft |
| 4.7 (TPS62736 only) | 2.0 x 2.5 x 1.2 | DFE252012R-H-4R7M | Toko |

10.2.1.2.2 Output Capacitor Selection

The output capacitor is chosen based on transient response behavior and ripple magnitude. The lower the capacitor value, the larger the ripple will become and the larger the droop will be in the case of a transient response. It is recommended to use at least a $22\text{-}\mu\text{F}$ output capacitor for most applications.

10.2.1.2.3 Input Capacitor Selection

The bulk input capacitance is recommended to be a minimum of $4.7 \mu\text{F} \pm 20\%$ for the TPS62736 and $22 \mu\text{F} \pm 20\%$ for the TPS62737. This bulk capacitance is used to suppress the lower frequency transients produced by the switching converter. There is no upper bound to the input-bulk capacitance. In addition, a high-frequency bypass capacitor of $0.1 \mu\text{F}$ is recommended in parallel with the bulk capacitor. The high-frequency bypass is used to suppress the high-frequency transients produced by the switching converter.

10.2.1.2.4 Resistor Selection

[Equation 1](#) to [Equation 4](#) are the equations for sizing the external resistors to set the V_{IN_OK} threshold and V_{OUT} regulation value. The spreadsheet at [SLVC489](#) can help size the external resistors.

10.2.1.3 Application Curves

See efficiency, line regulation, and load regulation curves at [Figure 30](#), [Figure 37](#), and [Figure 36](#).

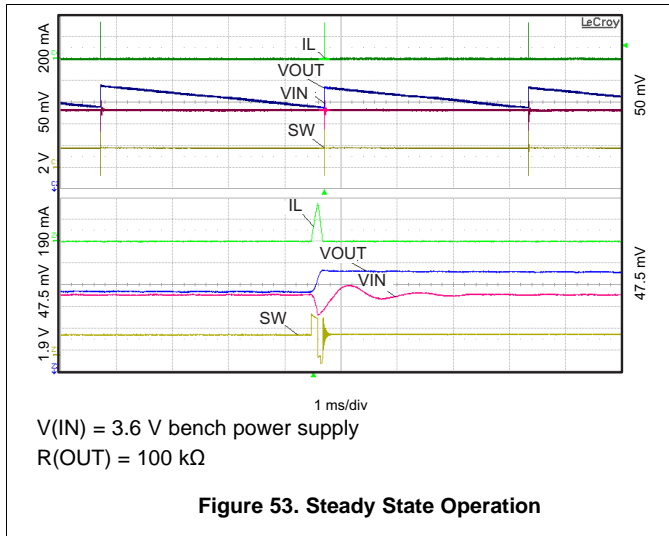


Figure 53. Steady State Operation

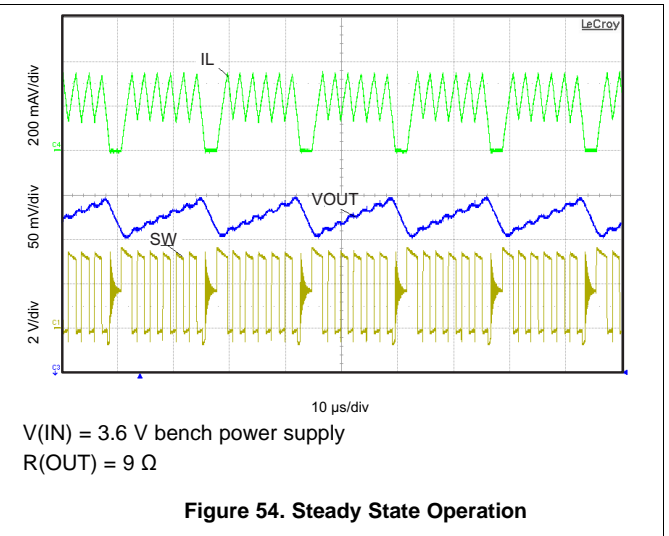


Figure 54. Steady State Operation

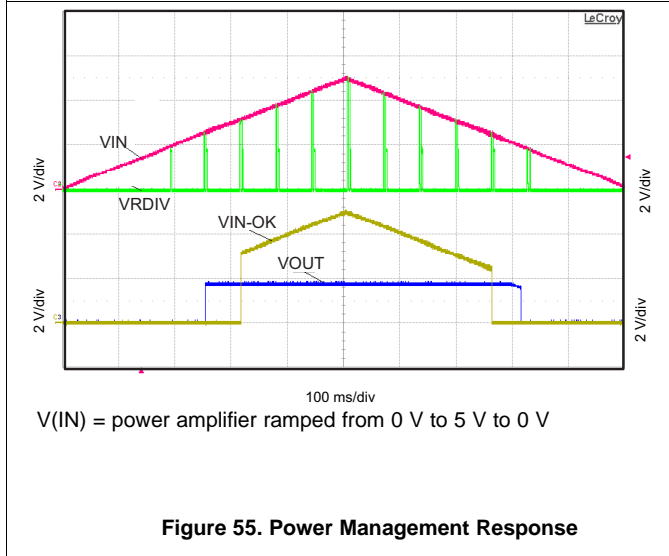


Figure 55. Power Management Response

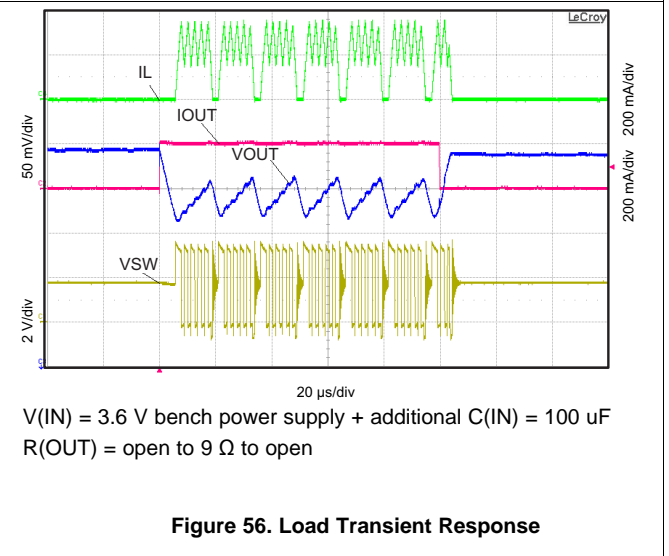


Figure 56. Load Transient Response

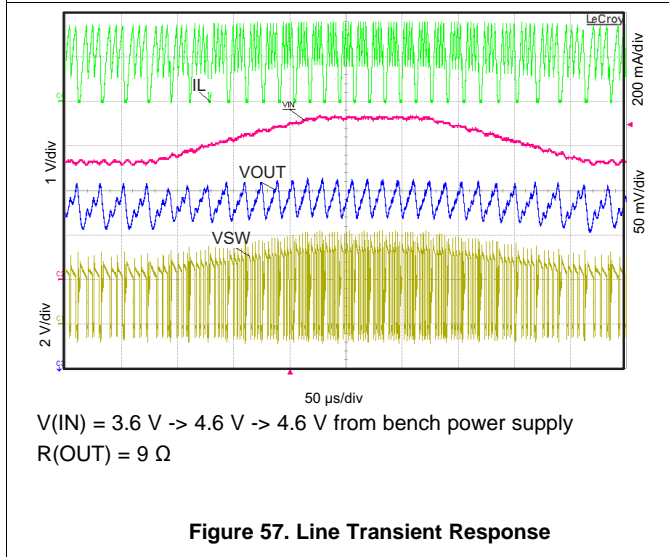


Figure 57. Line Transient Response

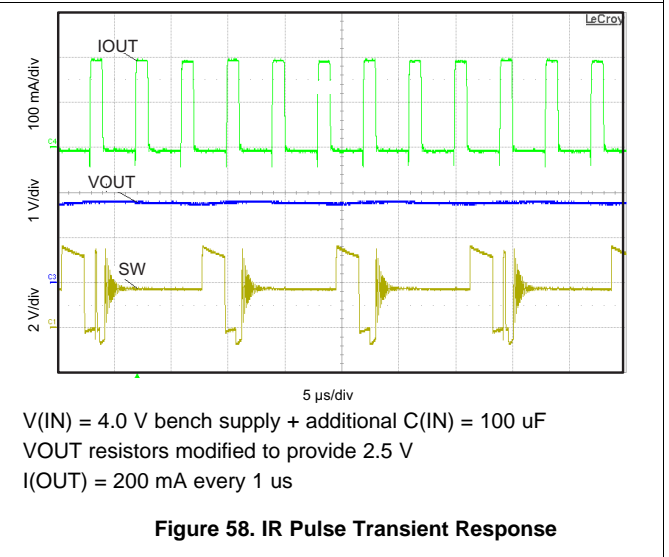
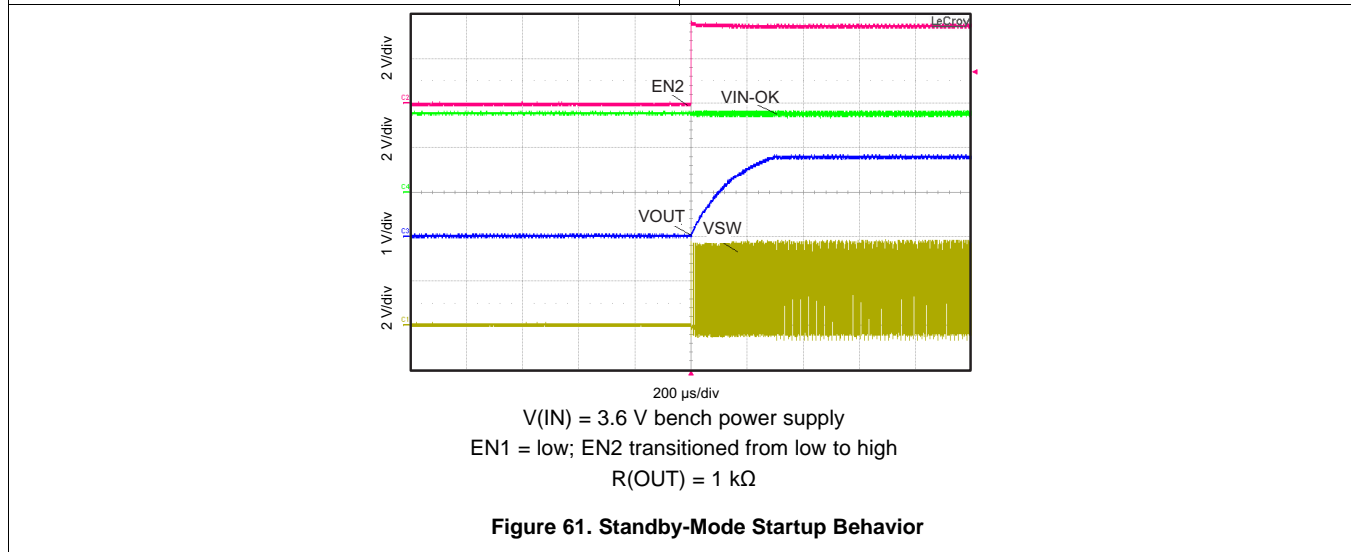
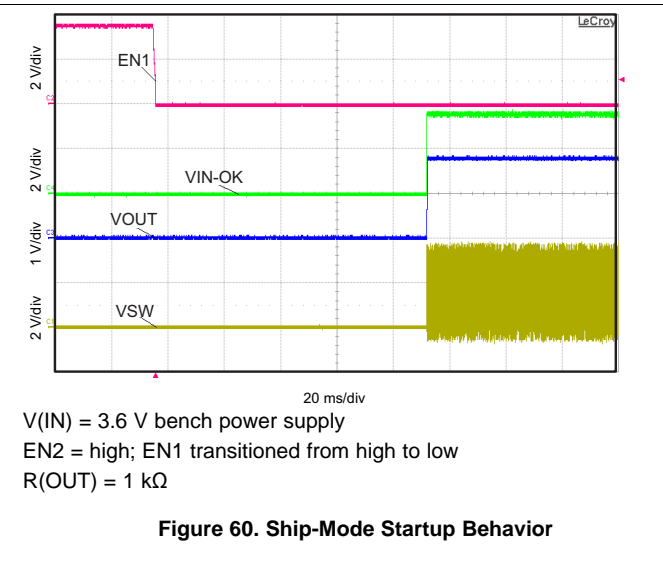
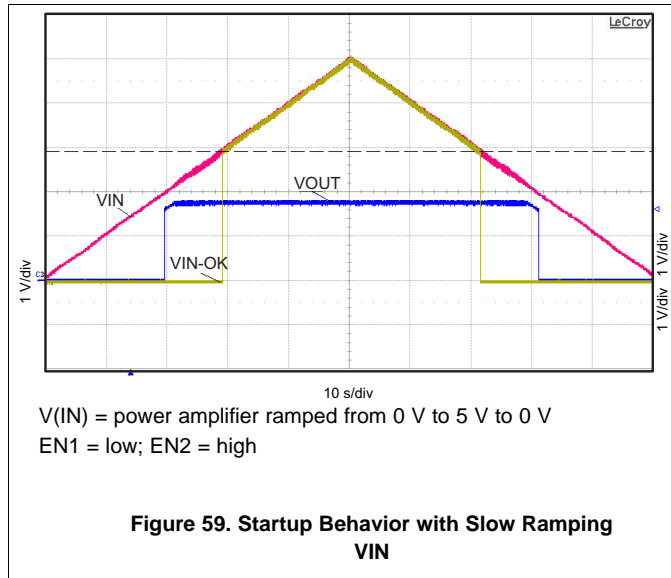


Figure 58. IR Pulse Transient Response



10.2.2 TPS62736 4-Resistor Typical Application Circuit

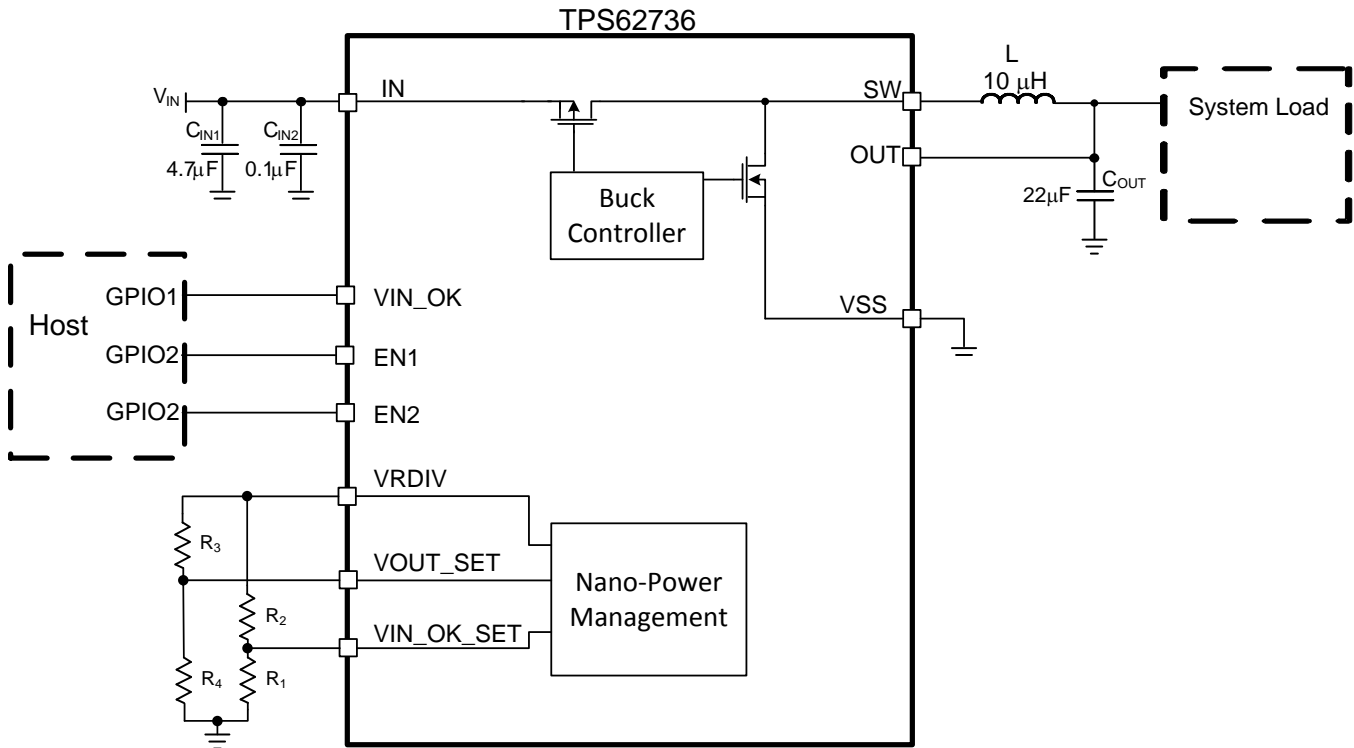


Figure 62. TPS62736 4-Resistor Typical Application Circuit

10.2.2.1 Design Requirements

A 2.5-V, up to 50-mA regulated power rail is needed. The VIN_OK comparator should indicate when the input voltage drops below 2.9 V. No large load transients are expected.

10.2.2.2 Detailed Design Procedure

The recommended 10-µH inductor (TOKO DFE252012C) and 4.7-µF input capacitor are used. Since no large load transients are expected, the minimum 22-µF output capacitor is used. Had a large load transient been expected, we would have sized the capacitor using $ITRAN = C_{OUT} \times \Delta V_{OUT} / \Delta TIME$ where ΔV_{OUT} is amount of VOUT droop allowed for the time of the transient.

First set $RSUM = R1 + R2 = R3 + R4 = 13 \text{ M}\Omega$ then solve Equation 4 for $R1 = V_{BIAS} \times RSUM / VIN_OK = 1.21 \text{ V} \times 13 \text{ M}\Omega / 2.9 \text{ V} = 5.42 \text{ M}\Omega \rightarrow 5.36 \text{ M}\Omega$ as the closest 1% resistor.

Then $R2 = RSUM - R1 = 13 \text{ M}\Omega - 5.42 \text{ M}\Omega = 7.58 \text{ M}\Omega \rightarrow 7.5 \text{ M}\Omega$ as the closest 1% resistor.

Solve Equation 3 for $R4 = V_{BIAS} \times RSUM / V_{OUT} = 1.21 \text{ V} \times 13 \text{ M}\Omega / 2.5 \text{ V} = 6.29 \text{ M}\Omega \rightarrow 6.34 \text{ M}\Omega$ as the closest 1% resistor.

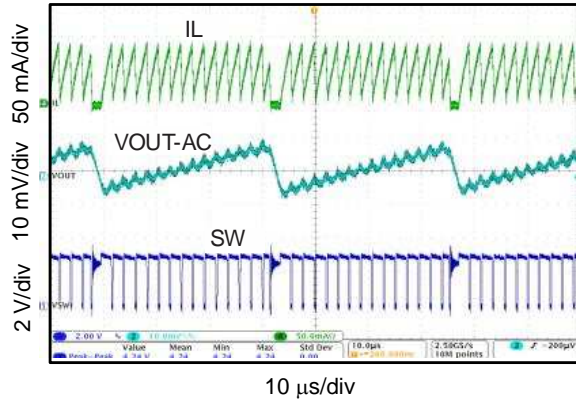
Finally $R3 = RSUM - R4 = 13 \text{ M}\Omega - 6.29 \text{ M}\Omega = 6.71 \text{ M}\Omega \rightarrow 6.81 \text{ M}\Omega$ as the closest 1% resistor.

These values yield $V_{OUT} = 2.51 \text{ V}$ and VIN_OK threshold = 2.90 V.

If using 3 resistors, see Resistor Selection for guidance on sizing the resistors.

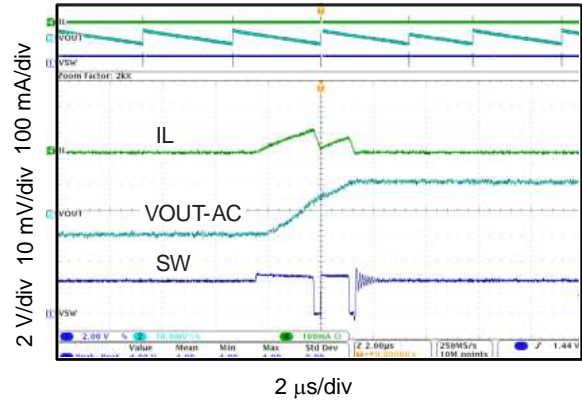
10.2.2.3 Application Curves

See efficiency, load regulation and line regulation graphs at Figure 1, Figure 7 and Figure 8 respectively.



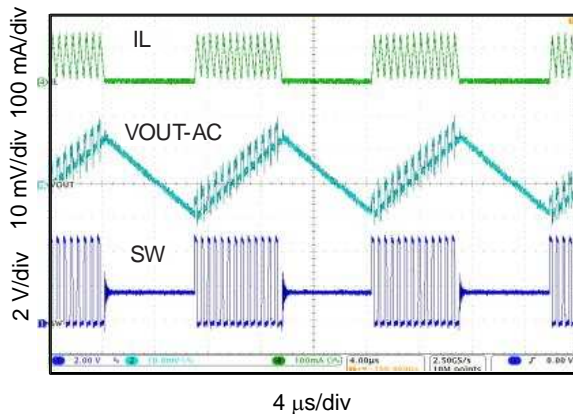
$V(IN) = 3.0\text{ V}$ bench power supply
 $R(OUT) = 50\ \Omega$

Figure 63. Steady State Operation



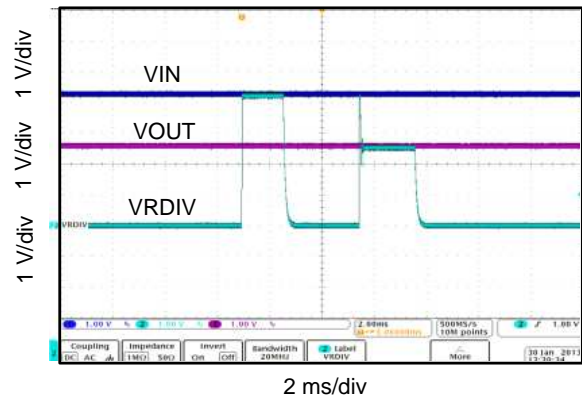
$V(IN) = 3.0\text{ V}$ bench power supply
 $R(OUT) = 100\ \text{k}\Omega$

Figure 64. Steady State Operation



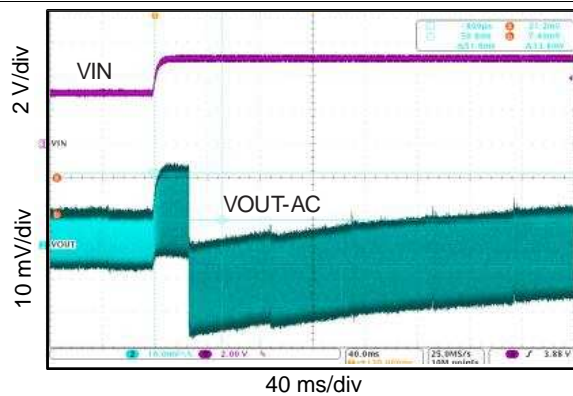
$V(IN) = 3.0\text{ V}$ bench power supply
 $VOUT$ resistors changed to provide 1.8 V ; $L = 4.7\ \mu\text{H}$
 $R(OUT) = 100\ \text{k}\Omega$

Figure 65. Steady State Operation



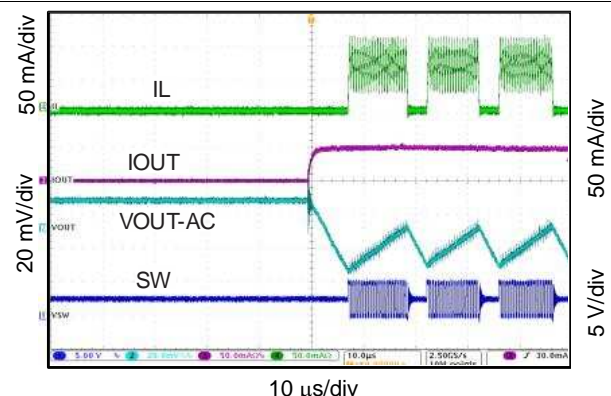
$V(IN) = 3.0\text{ V}$ bench power supply

Figure 66. Sampling Waveform



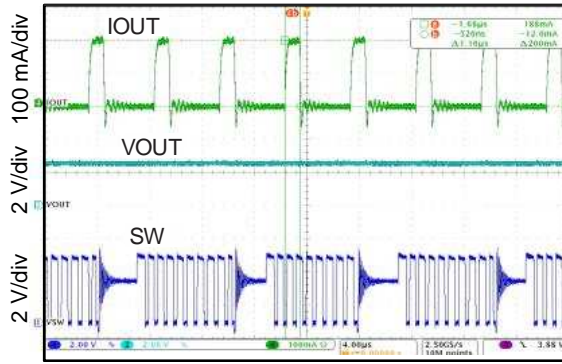
$V(IN) = 3.0\text{ V} \rightarrow 5.0\text{ V}$ from bench power supply
 $R(OUT) = 50\ \Omega$

Figure 67. Line Transient Response



$V(IN) = 4.0\text{ V}$ from bench power supply + additional $CIN = 100\ \mu\text{F}$
 $R(OUT) = \text{open} \rightarrow 50\ \Omega$

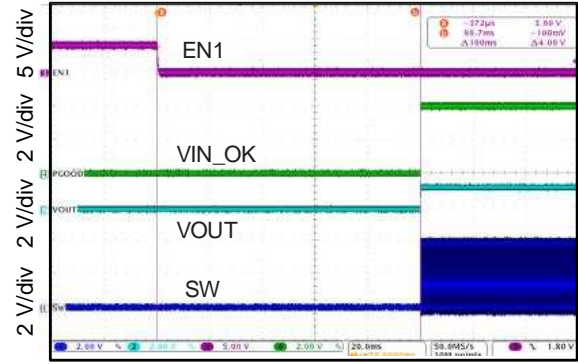
Figure 68. Load Transient Response



4 μ s/div

V(IN) = 4.0 V from bench power supply + additional CIN = 100 μ F
I(OUT) = 200 mA every 1 μ s

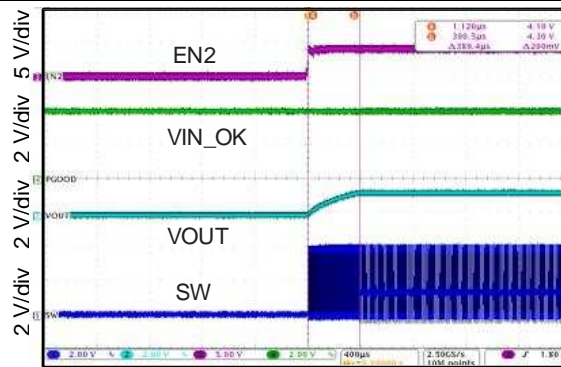
Figure 69. IR Pulse Transient Response



20 ms/div

V(IN) = 4.0 V from bench power supply
VOUT resistors modified to provide 1.8 V
EN2 = high, EN1 transitioned high to low

Figure 70. Ship-Mode Startup Behavior



400 μ s/div

V(IN) = 4.0 V from bench power supply
VOUT resistors modified to provide 1.8 V
EN1 = low, EN2 transitioned low to high

Figure 71. Standby-Mode Startup Behavior

11 Power Supply Recommendations

The TPS62736 / 7 ICs require a low impedance power source (e.g. battery, wall adapter) capable of providing between 2.0 V and 5.5 V and up to 100 mA / 370 mA respectively. When the voltage at IN is less than or equal to VOUT, the IC stops switching, turns on the high side FET and provides $V_{OUT} = V_{IN} - I_{LOAD} \times R_{DS(on)-HighSideFET}$.

12 Layout

12.1 Layout Guidelines

To minimize switching noise generation, the step-down converter (buck) power stage external components must be carefully placed. The most critical external component for a buck power stage is its input capacitor. The bulk input capacitor (C_{IN1}) and high frequency decoupling capacitor (C_{IN2}) must be placed as close as possible between the power stage input (IN pin 1) and ground (VSS pin 12). Next, the inductor (L1) must be placed as close as possible between the switching node (SW pin 13) and the output voltage (OUT pin 11). Finally, the output capacitor (C_{OUT}) should be placed as close as possible between the output voltage (OUT pin 11) and GND (VSS pin 12). In the diagram below, the input and output capacitor grounds are connected to VSS pin 12 through vias to the bottom-layer ground plane of the PCB.

To minimize noise pickup by the high impedance voltage setting nodes (VIN_OK_SET pin 8 and VOUT_SET pin 9), the external resistors (R1, R2 and R3) should be placed so that the traces connecting the midpoints of the string are as short as possible. In the diagram below, the connection to VOUT_SET is by a bottom layer trace.

The remaining pins are either NC pins, that should be connected to the PowerPAD™ as shown below, or digital signals with minimal layout restrictions.

In order to maximize efficiency at light load, the use of voltage level setting resistors $> 1\text{ M}\Omega$ is recommended. However, during board assembly, contaminants such as solder flux and even some board cleaning agents can leave residue that may form parasitic resistors across the physical resistors and/or from one end of a resistor to ground, especially in humid, fast airflow environments. This can result in the voltage regulation and threshold levels changing significantly from those expected per the installed resistor values. Therefore, it is highly recommended that no ground planes be poured near the voltage setting resistors. In addition, the boards must be carefully cleaned, possibly rotated at least once during cleaning, and then rinsed with de-ionized water until the ionic contamination of that water is well above 50 MΩ. If this is not feasible, then it is recommended that the sum of the voltage setting resistors be reduced to at least 5 times below the measured ionic contamination.

12.2 Layout Example

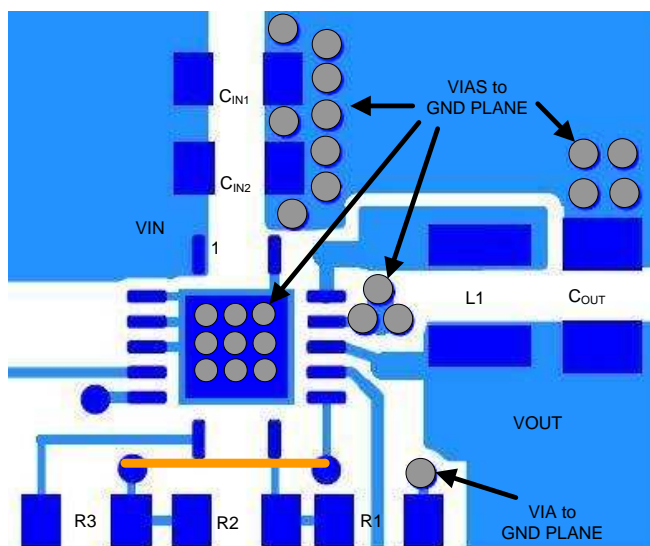


Figure 72. Recommended Layout, TPS62736

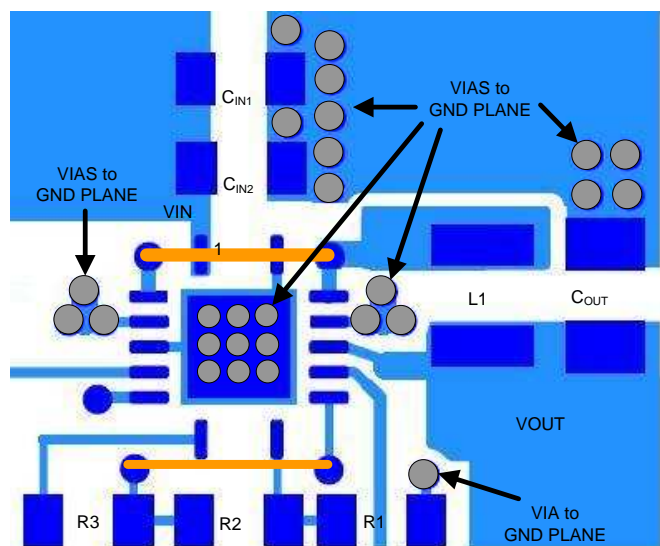


Figure 73. Recommended Layout, TPS62737

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TPS62736 | Click here | Click here | Click here | Click here | Click here |
| TPS62737 | Click here | Click here | Click here | Click here | Click here |

13.3 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS62736RGYR | ACTIVE | VQFN | RGY | 14 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 62736 | Samples |
| TPS62736RGYT | ACTIVE | VQFN | RGY | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 62736 | Samples |
| TPS62737RGYR | ACTIVE | VQFN | RGY | 14 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 0 | 62737 | Samples |
| TPS62737RGYT | ACTIVE | VQFN | RGY | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 0 | 62737 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

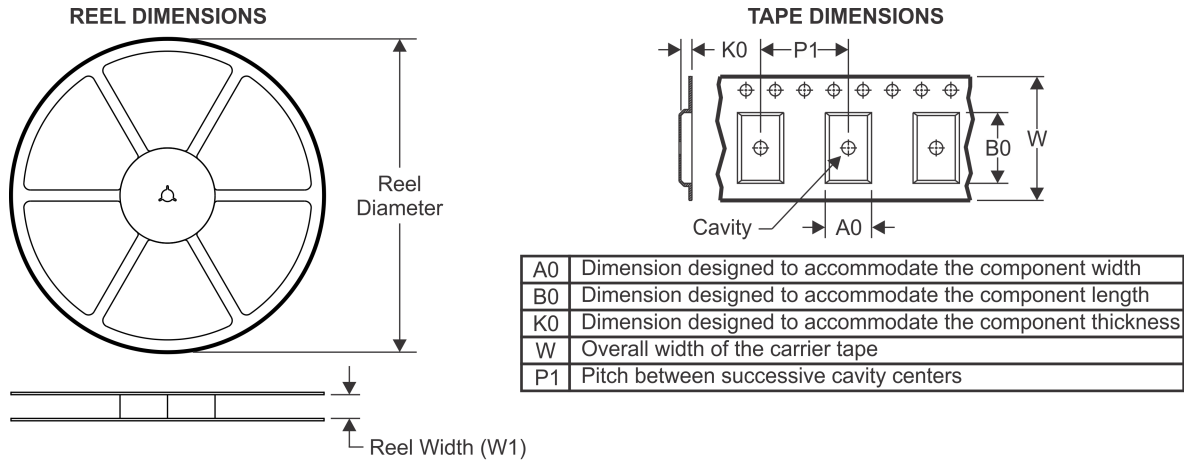
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS62736RGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS62736RGYT | VQFN | RGY | 14 | 250 | 180.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS62737RGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q2 |
| TPS62737RGYT | VQFN | RGY | 14 | 250 | 180.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q2 |

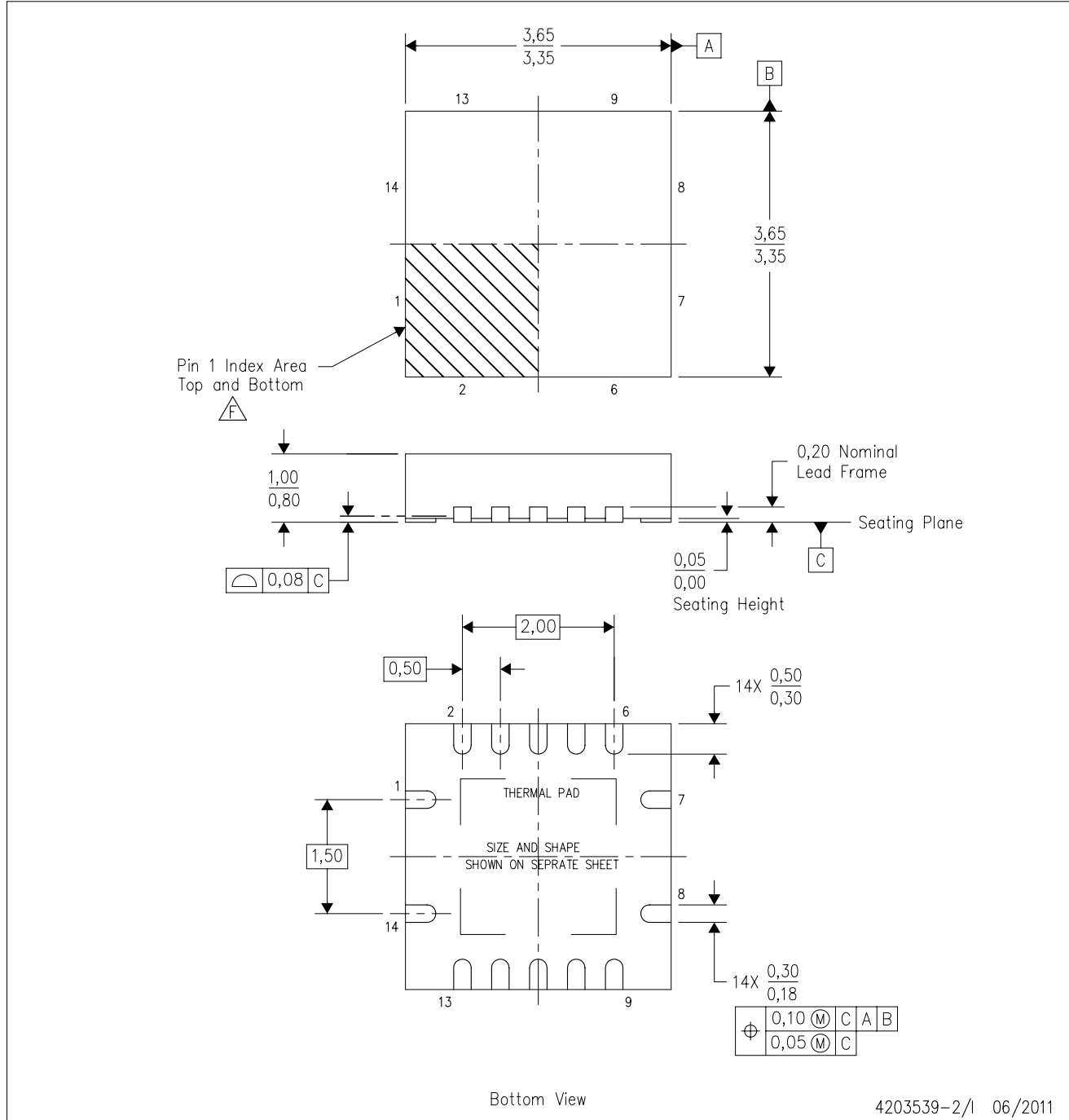
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS62736RGYR | VQFN | RGY | 14 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS62736RGYT | VQFN | RGY | 14 | 250 | 210.0 | 185.0 | 35.0 |
| TPS62737RGYR | VQFN | RGY | 14 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS62737RGYT | VQFN | RGY | 14 | 250 | 210.0 | 185.0 | 35.0 |

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

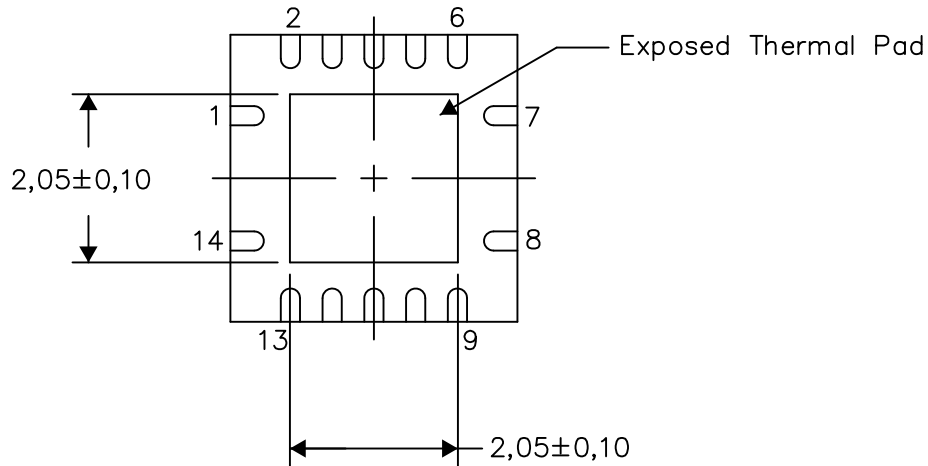
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

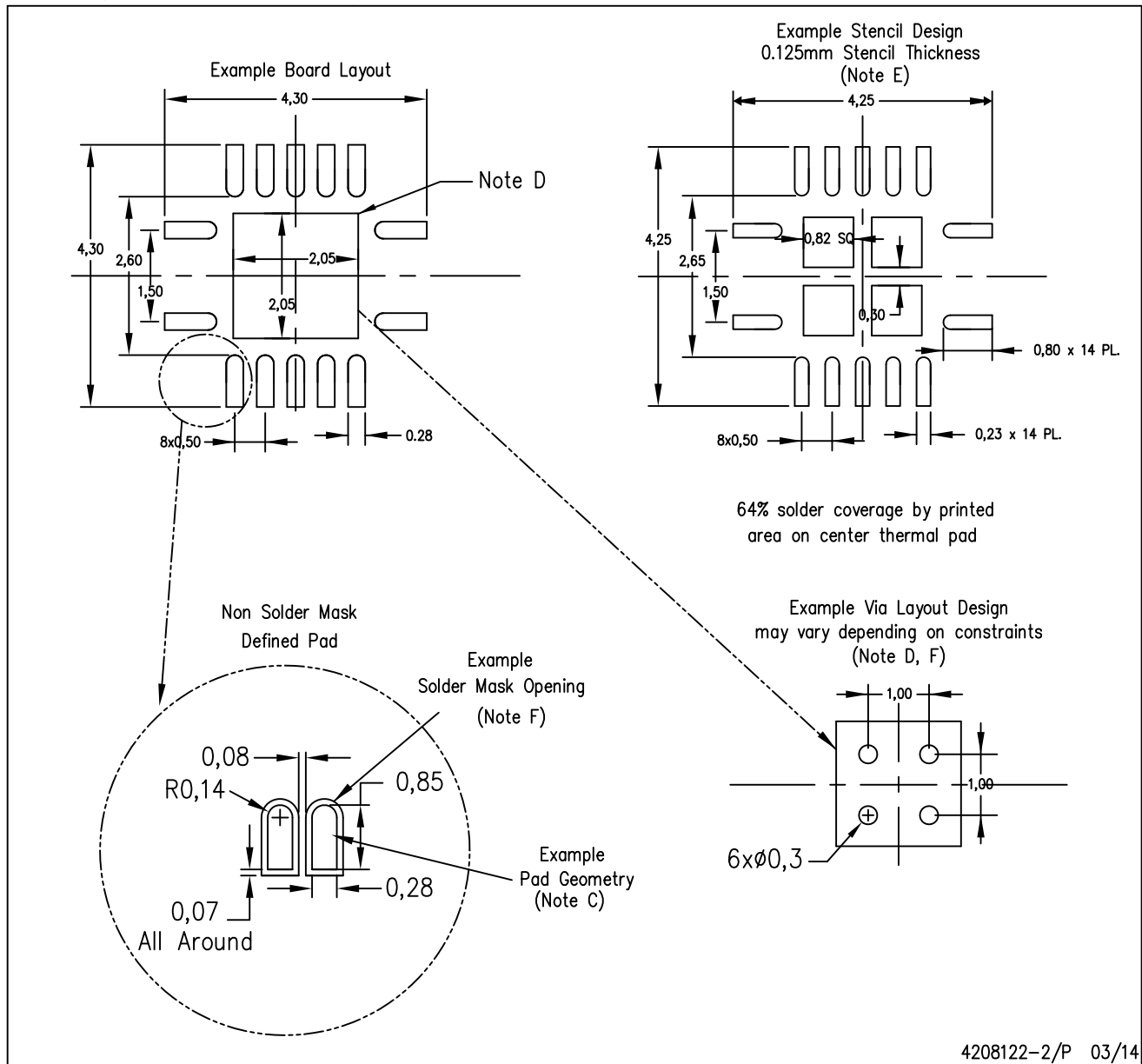
Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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