60V High Current Step-Down LED Driver Controller

FEATURES

- **Accurately Control Input and Output Current**
- **3000:1 True Color PWM™ Dimming**
- **±1.5% Voltage Regulation Accuracy**
- **±6% Current Regulation Accuracy**
- 6V to 60V Input Voltage Range
- Wide Output Range Up to 55V
- <2µA Shutdown Current
- Control Pin for Thermal Control of Load Current
- Input and Output Current Monitor and Limit
- Open, Short, and C/10 Fault Detection
- PWM Driver Output for LED Applications
- Thermally Enhanced 28-Lead FE Package

APPLICATIONS

- High Power Architectural Lighting
- Automotive Lighting
- Aviation and Marine Strobe Lights
- Solar-Powered Chargers, Laser Diodes

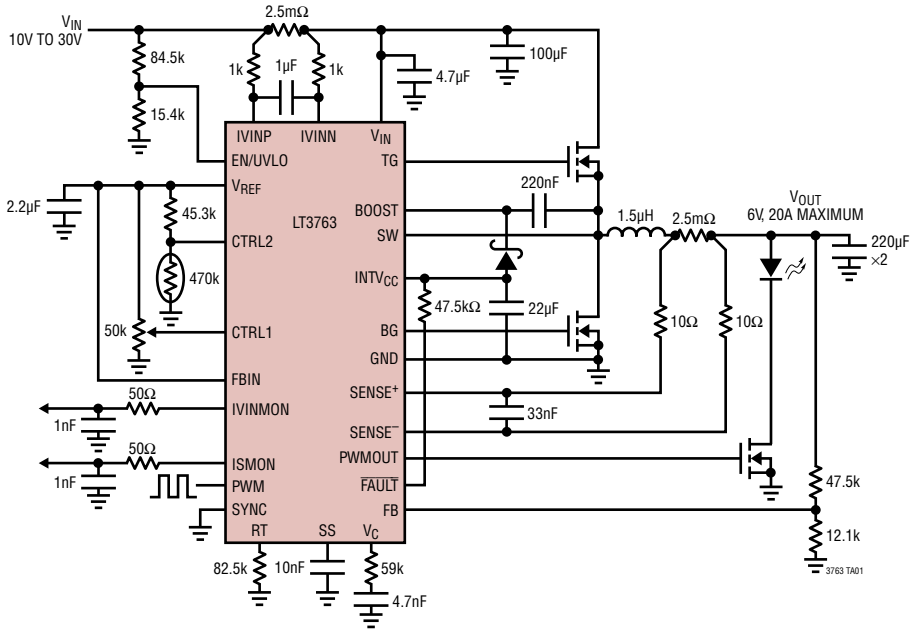
DESCRIPTION

The LT®3763 is a fixed frequency, synchronous, step-down DC/DC controller designed to accurately regulate output currents up to 20A. The average current mode controller will maintain inductor current regulation over a wide output voltage range from 0V to 55V. Output current is set by analog voltages on the CTRL pins and an external sense resistor. Voltage regulation and overvoltage protection are set with a voltage divider from the output to the FB pin. The switching frequency is programmable from 200kHz to 1MHz through an external resistor on the RT pin or with the SYNC pin and an external clock signal. Input and output current sensing provides input current limiting and an accurate measurement of these currents. The FBIN pin is provided for applications requiring a peak power tracking function.

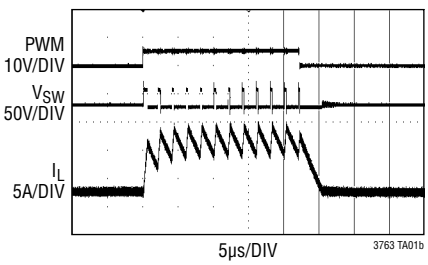
Additional features include an accurate external reference voltage for use with the CTRL pins, an accurate UVLO/EN pin that allows for programmable UVLO hysteresis, a PWM driver for LED applications, output voltage fault detection, and thermal shutdown.

TYPICAL APPLICATION

20A, Pulse Width Modulated, Single LED Driver



PWM Dimming



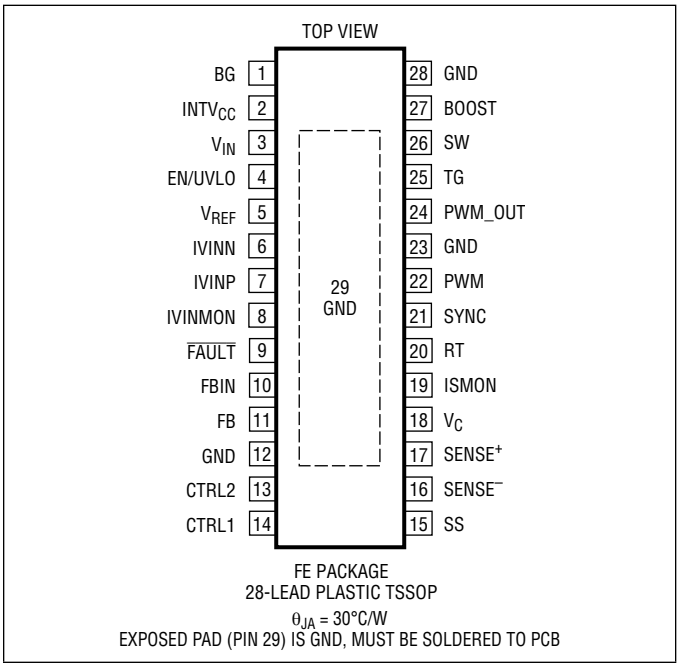
Rev. C

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, EN/UVLO, IVINP, and IVINN 60V
$SENSE^+$ and $SENSE^-$ 60V
CTRL1, CTRL2, FB, and FBIN 3V
SYNC and PWM 6V
$INTV_{CC}$ and $\overline{FAULT}$ 6V
V_C, RT, and SS 3V
V_{REF}, IVINMON, and ISMON 3V
SW 60V
BOOST 66V
BOOST-SW 6V
Operating Junction Temperature (Notes 2, 3)
LT3763E/LT3763I ..... –40°C to 125°C
LT3763H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



FE PACKAGE
28-LEAD PLASTIC TSSOP
θ_{JA} = 30°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3763EFE#PBF	LT3763EFE#TRPBF	LT3763FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3763IFE#PBF	LT3763IFE#TRPBF	LT3763FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3763HFE#PBF	LT3763HFE#TRPBF	LT3763FE	28-Lead Plastic TSSOP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $V_{EN/UVLO}$ = 5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			6		60	V
Supply Undervoltage Lockout	From Low to High		3.75	4.0	4.25	V
V_{IN} Pin Quiescent Current Non-Switching Operation Shutdown Mode	 $V_{EN/UVLO}$ = 1.4V, Not Switching $V_{EN/UVLO}$ = 0V			 1.7 0.2	 3.5 2	 mA µA
EN/UVLO Pin Threshold (Falling Edge)			1.47	1.52	1.57	V
EN/UVLO Hysteresis				185		mV
EN/UVLO Pin Current	EN/UVLO = 1.4V, V_{IN} = 6V			5		µA
SYNC Pin Threshold (Falling Edge)			1.4	1.5	1.6	V
SYNC Pin Hysteresis				675		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $V_{EN/UVLO}$ = 5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PWM Pin Threshold (Falling Edge)			1.4	1.5	1.6	V
PWM Pin Hysteresis				675		mV
CTRL1 Pin Current	V_{CTRL1} = 1.5V			20		nA
CTRL2 Pin Current	V_{CTRL1} = 1.5V, V_{CTRL2} = 1.5V, V_{FBIN} = 2V			100		nA
Reference						
Reference Voltage (V_{REF} pin)		●	1.94	2	2.06	V
Inductor Current Sensing						
Full Range SENSE+ to SENSE–	V_{CTRL1} = 2V, V_{CTRL2} > 2V, V_{SS} = V_{FBIN} = 2V, V_C = 1.2V	●	48	51	54	mV
SENSE+ Pin Current	V_{SENSE^+} = V_{SENSE^-} = 4V			–20		µA
SENSE– Pin Current	V_{SENSE^+} = V_{SENSE^-} = 4V, V_{CTRL1} = 1.5V			–40		µA
Internal V_{CC} Regulator ($INTV_{CC}$ Pin)						
Regulation Voltage	I_{LOAD} = 10mA	●	4.8	5	5.2	V
Current Limit	V_{INTVCC} = 0V			60		mA
NMOS FET Driver						
Non-Overlap Time TG to BG				42		ns
Non-Overlap Time BG to TG				44		ns
Minimum On-Time BG	(Note 4)			50		ns
Minimum On-Time TG	(Note 4)			55		ns
Minimum Off-Time BG	(Note 4)			140		ns
High Side Driver Switch On-Resistance Gate Pull-Up Gate Pull-Down	V_{CBOOST} – V_{SW} = 5V			 2.2 1.3		 Ω Ω
Low Side Driver Switch On-Resistance Gate Pull-Up Gate Pull-Down	V_{INTVCC} = 5V			 2.2 1		 Ω Ω
Switching Frequency	R_T = 40kΩ R_T = 221kΩ	●	930 180	1000 200	1070 220	kHz kHz
Soft-Start						
Charging Current				11		µA
Voltage Regulation Amplifier						
Input Bias Current	V_{FB} = 1.3V			750		nA
g_m				850		µA/V
Feedback Regulation Voltage	V_{SENSE^+} = V_{SENSE^-} = V_{CTRL1} = 2V	●	1.188	1.206	1.224	V
FAULT Comparator						
Upper FAULT Threshold (FB Rising)		●	1.137	1.16	1.183	V
Upper FAULT Threshold Hysteresis				40		mV
Lower FAULT Threshold (FB Falling)		●	0.24	0.25	0.265	V
Lower FAULT Threshold Hysteresis				40		mV
$\overline{FAULT}$ Pull-Down Current	$V_{\overline{FAULT}}$ = 2V, V_{FB} = 0V			8		mA
Input Voltage Regulation						
FBIN Pin Current	V_{FBIN} = 1.5V			150		nA
Sense Voltage (V_{SENSE^+} – V_{SENSE^-})	V_{FBIN} = 1.22V, V_{SENSE^-} = 4V V_{FBIN} = 1.26V, V_{SENSE^-} = 4V			10 45		mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $V_{EN/UVLO}$ = 5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Current Monitor						
Sense Voltage ($V_{SENSE}^+ – V_{SENSE}^–$)	V_{ISMON} Regulated to 1V, $V_{SENSE}^–$ = 10V V_{ISMON} Regulated to 200mV, $V_{SENSE}^–$ = 10V		45 5	50 10	55 15	mV mV
Input Current Monitor						
Sense Voltage ($V_{IVIN}^+ – V_{IVIN}^–$)	$V_{IVINMON}$ Regulated to 1V, V_{IVIN}^+ = 12V $V_{IVINMON}$ Regulated to 200mV, V_{IVIN}^+ = 12V		46 6	50 10	54 14	mV mV
Input Current Limit Sense Voltage ($V_{IVIN}^+ – V_{IVIN}^–$)		●	45	50	55	mV
PWM Driver						
PWM_OUT Driver On-Resistance Gate Pull-Up Gate Pull-Down	V_{INTVCC} = 5V			 2.2 0.9		 Ω Ω
PWM to PWM_OUT Propagation Delay Rising Falling	V_{INTVCC} = 5V			 11 38		 ns ns
Current Control Loop g_m Amp						
Offset Voltage	$V_{SENSE}^–$ = 4V, V_{CTRL1} = 0V	●	–3	0	3	mV
Input Common Mode Range $V_{CM(LOW)}$ $V_{CM(HIGH)}$	 (Note 5) $V_{CM(HIGH)}$ Measured from V_{IN} to V_{CM}, $V_{SENSE}^+ = V_{SENSE}^–$			 0 1.4		 V V
Output Impedance				3.5		MΩ
g_m		●	375	475	625	µA/V
Differential Gain				1.7		V/mV
Overvoltage						
FB Overvoltage Protection (V_{FB} Maximum)				1.515		V
Overcurrent						
Overcurrent Protection ($V_{SENSE}^+ – V_{SENSE}^–$ Maximum)	$V_{SENSE}^–$ = 0V, R_T = 221kΩ			85		mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3763E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3763I is guaranteed to meet performance specifications over the –40°C to 125°C operating junction temperature range. The LT3763H is guaranteed over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C.

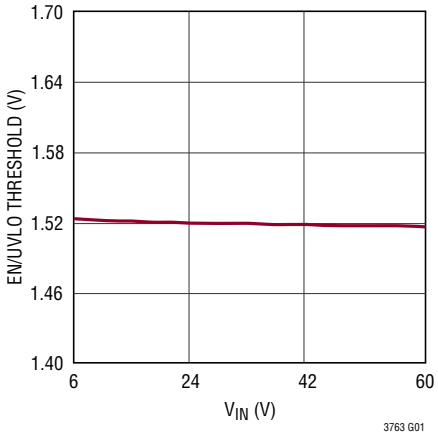
Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: The minimum on- and off-times are guaranteed by design and are not tested.

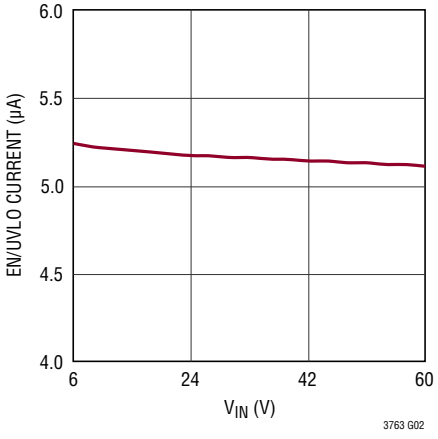
Note 5: The minimum common mode voltage is guaranteed by design and is not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

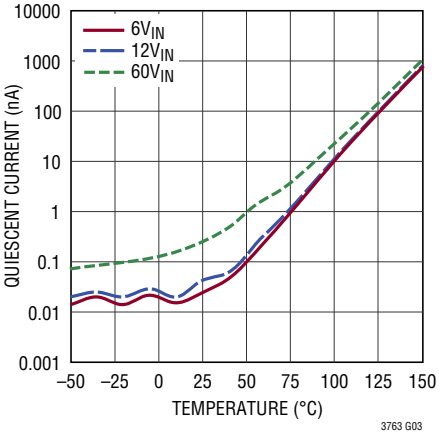
EN/UVLO Threshold (Falling)



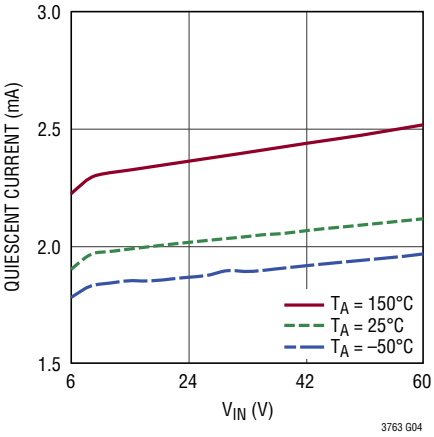
EN/UVLO Current



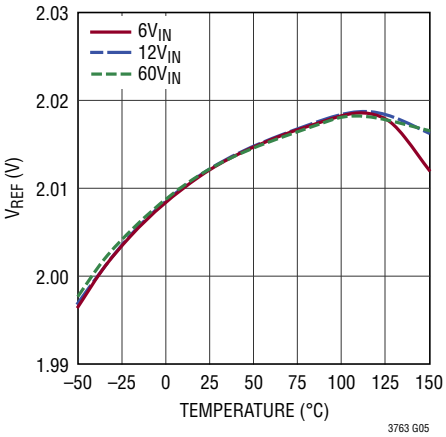
Quiescent Current (Shutdown)



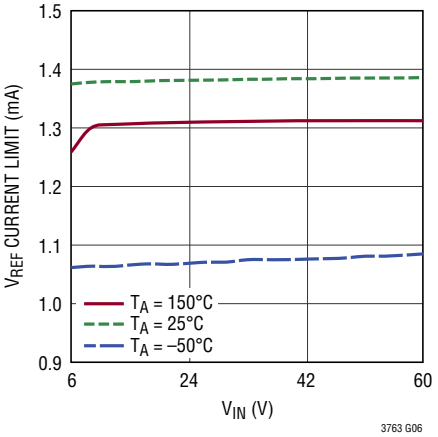
Quiescent Current (Non-Switching)



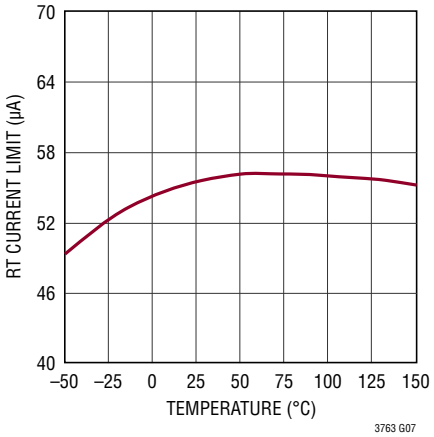
V_{REF} Voltage



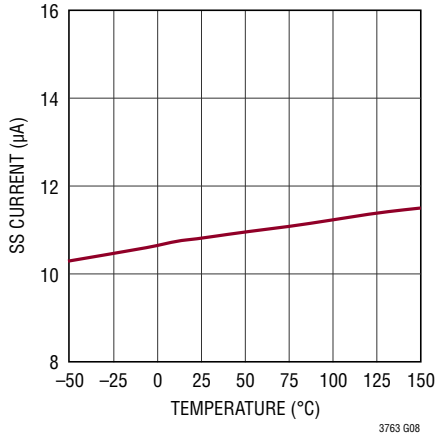
V_{REF} Current Limit



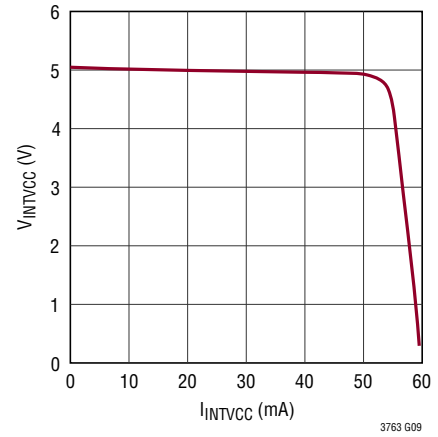
RT Current Limit



SS Current

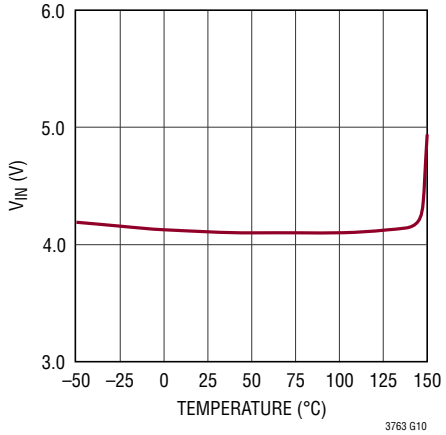


$INTV_{CC}$ Current Limit

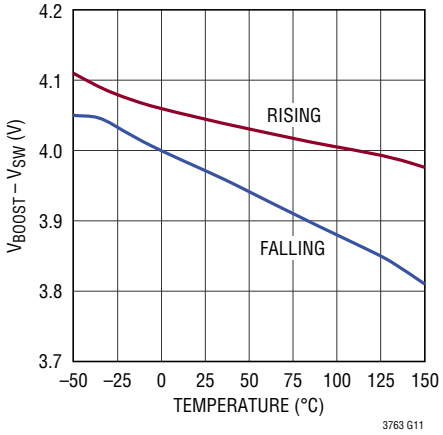


TYPICAL PERFORMANCE CHARACTERISTICS

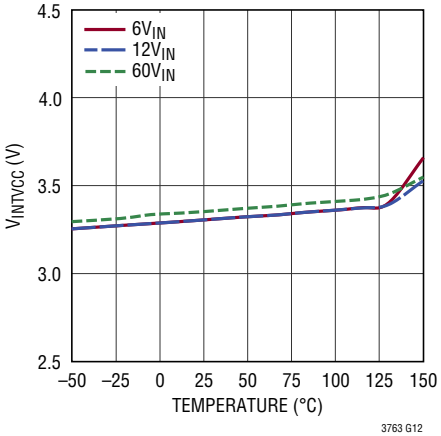
V_{IN} UVLO



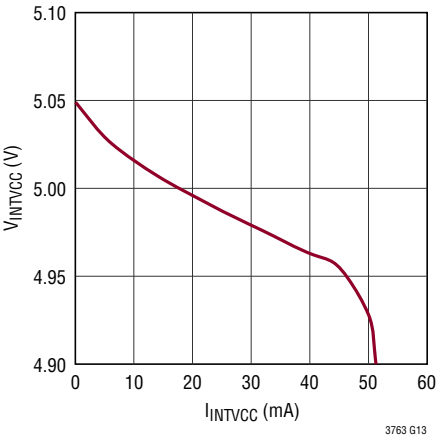
$V_{BOOST} – V_{SW}$ UVLO Thresholds



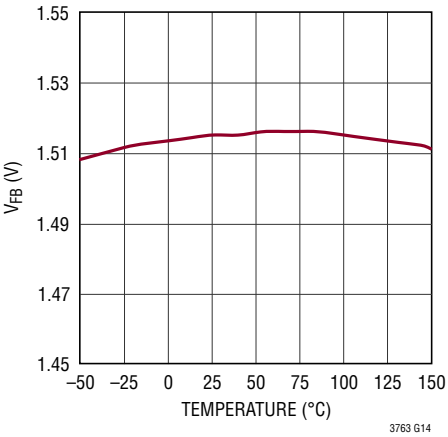
$INTV_{CC}$ UVLO



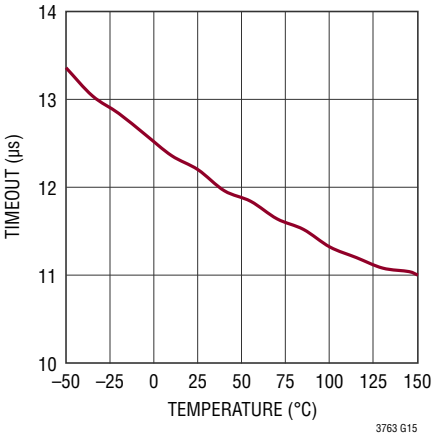
$INTV_{CC}$ Load Regulation



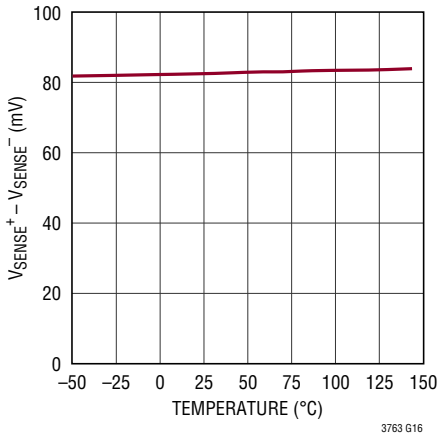
Overvoltage Threshold



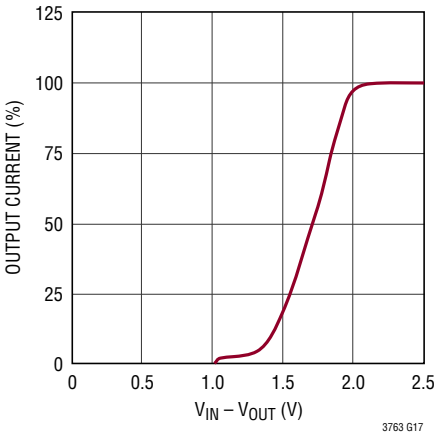
Overvoltage Timeout



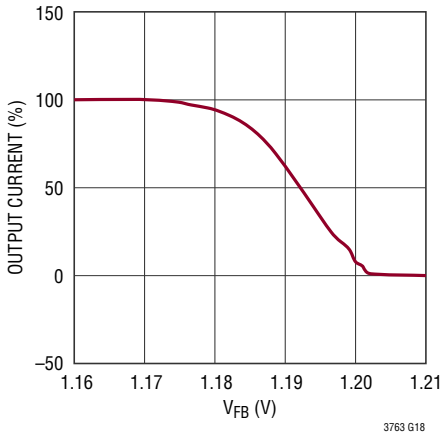
Overcurrent Threshold



Maximum Output Voltage

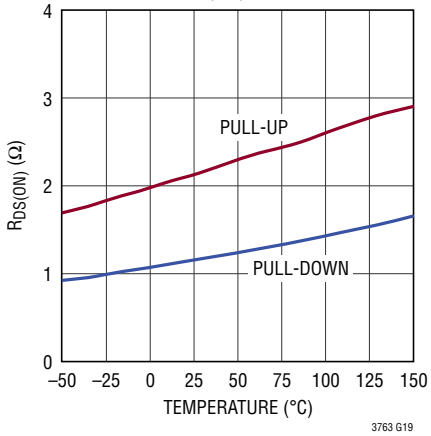


Regulated Current vs V_{FB}

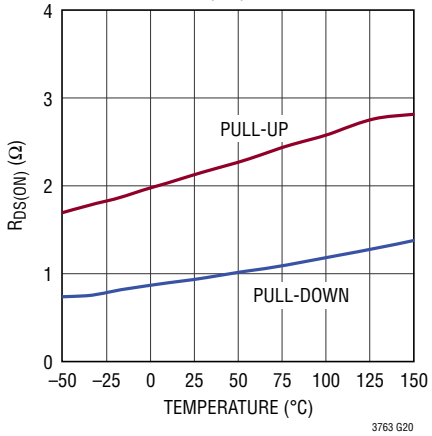


TYPICAL PERFORMANCE CHARACTERISTICS

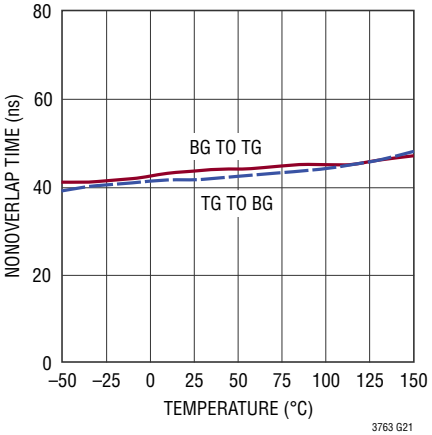
TG Driver $R_{DS(ON)}$



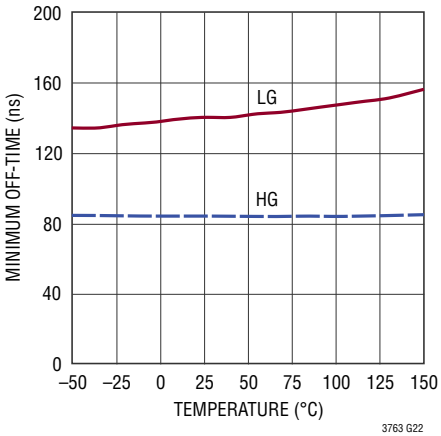
BG Driver $R_{DS(ON)}$



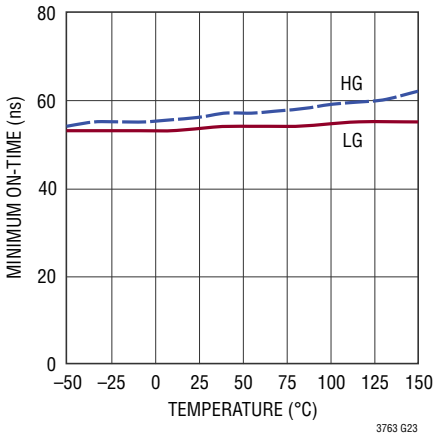
Nonoverlap Time



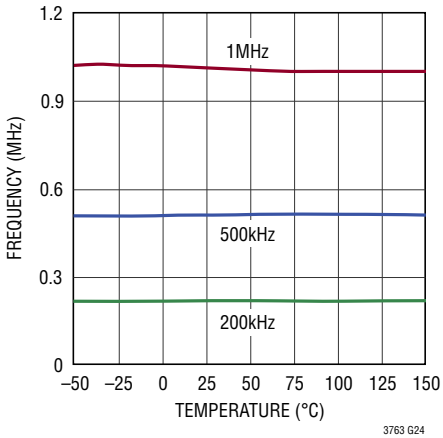
Minimum Off-Time



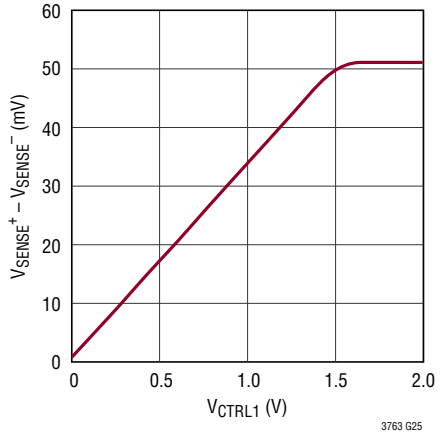
Minimum On-Time



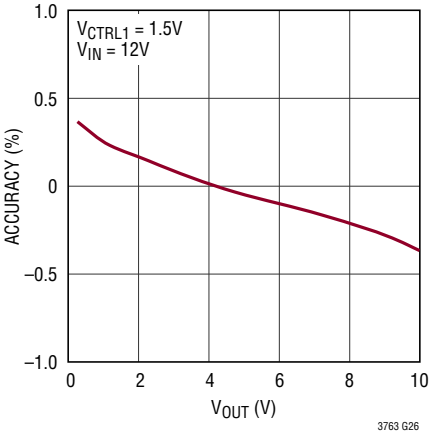
Oscillator Frequency



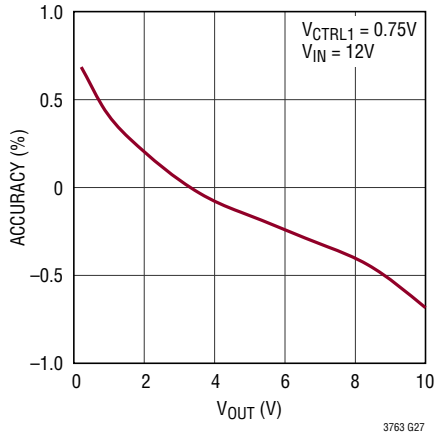
Regulated Sense Voltage



Current Regulation Accuracy

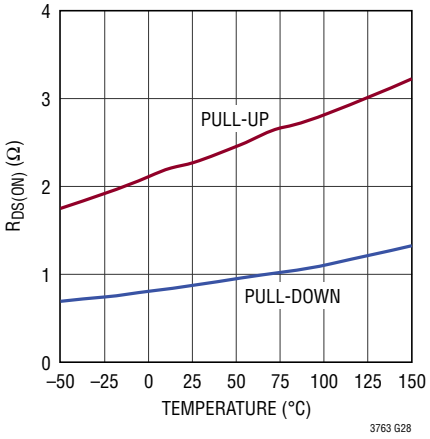


Current Regulation Accuracy

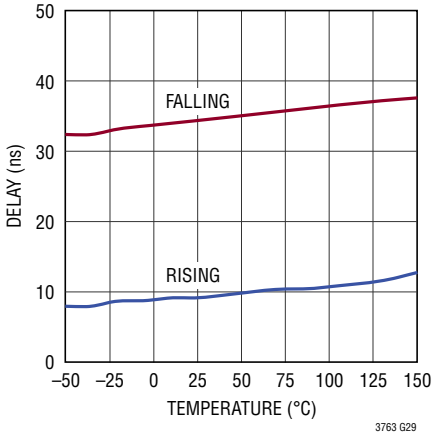


TYPICAL PERFORMANCE CHARACTERISTICS

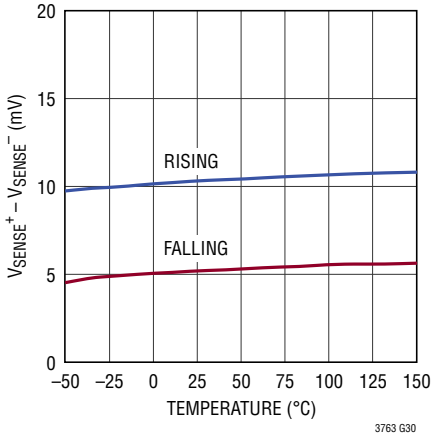
PWM Driver $R_{DS(ON)}$



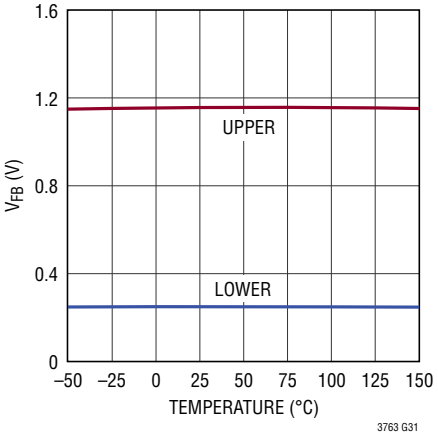
PWM Driver Delay



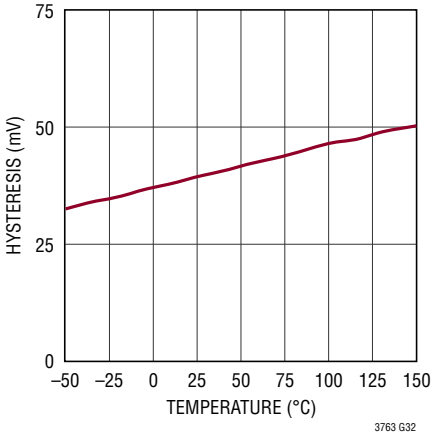
C/10 Threshold



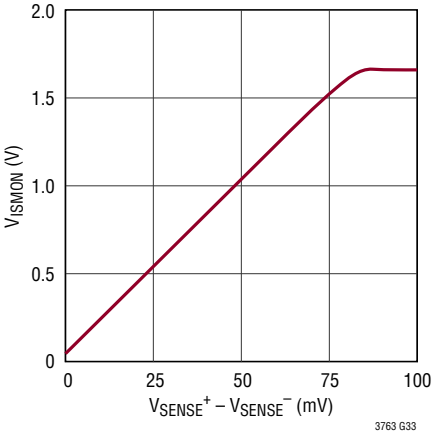
$\overline{\text{FAULT}}$ Threshold



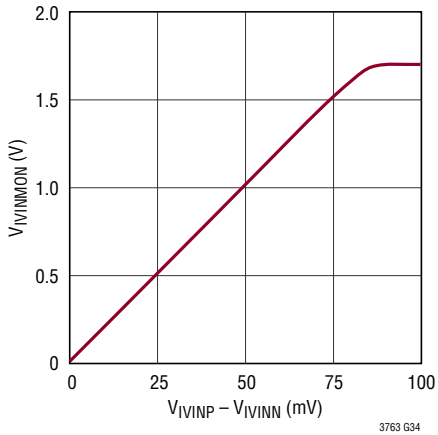
$\overline{\text{FAULT}}$ Hysteresis



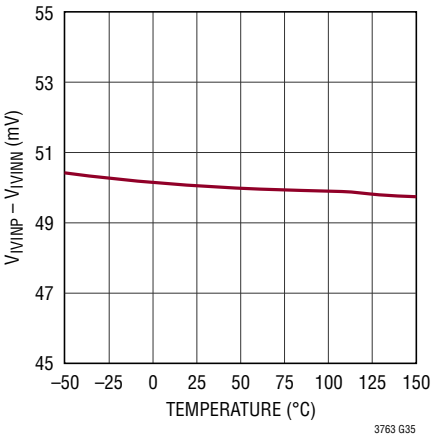
Output Current Sense



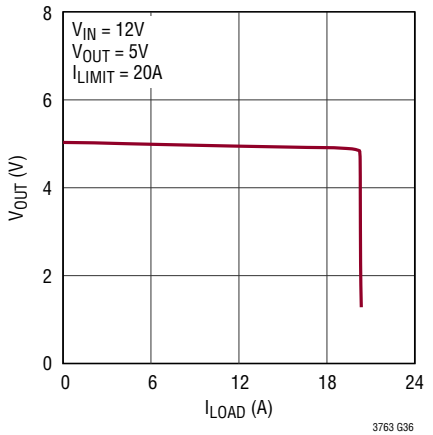
Input Current Sense



Input Current Limit

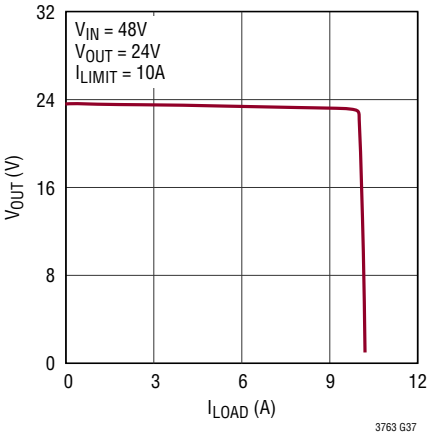


Output Voltage Load Regulation

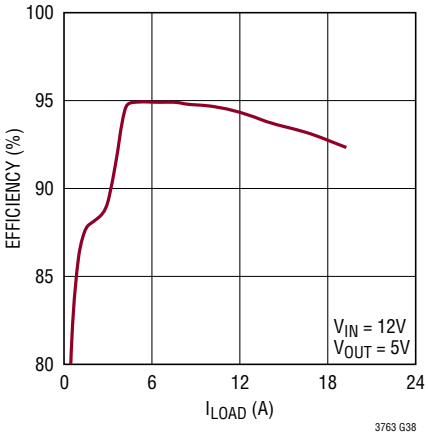


TYPICAL PERFORMANCE CHARACTERISTICS

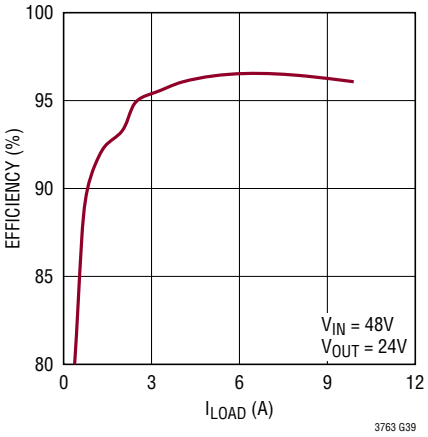
Output Voltage Load Regulation



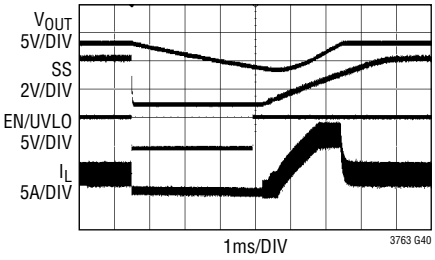
Efficiency vs Load Current



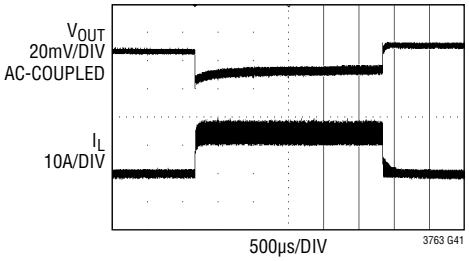
Efficiency vs Load Current



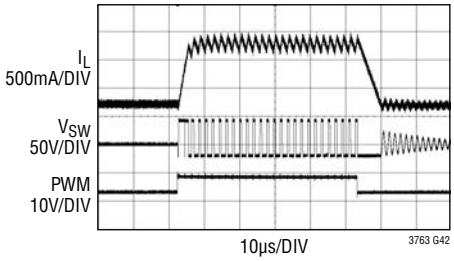
Shutdown and Recovery



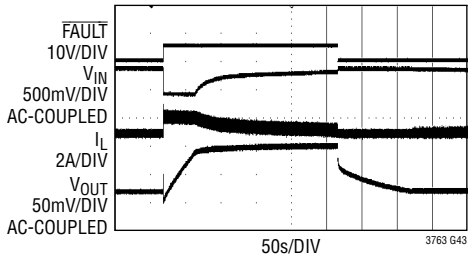
15A Load Step



PWM Dimming



Solar Powered SLA Battery Charging



PIN FUNCTIONS

BG (Pin 1): BG is the bottom FET gate drive signal that controls the state of the external low side power FET. The driver pull-up impedance is 2.2Ω, and pull-down impedance is 1Ω. Do not force any voltage on this pin.

$INTV_{CC}$ (Pin 2): The $INTV_{CC}$ pin provides a regulated 5V output for charging the BOOST capacitor. $INTV_{CC}$ also provides the power for the digital and switching subcircuits. Do not force any voltage on this pin. Bypass with at least a 22µF capacitor to ground. $INTV_{CC}$ is current-limited to 50mA. Shutdown operation disables the output voltage drive.

V_{IN} (Pin 3): Input Supply Pin. Must be locally bypassed with at least a 4.7µF low ESR capacitor to ground as close as possible to the exposed pad of the package.

EN/UVLO (Pin 4): Enable Pin. The EN/UVLO pin acts as an enable pin and turns on the internal current bias core and sub-regulators at 1.705V and turns off at 1.52V. The pin does not have any pull-up or pull-down, requiring a voltage bias for normal operation. Full shutdown occurs at approximately 0.5V. If unused, the Enable pin may be tied to V_{IN}.

V_{REF} (Pin 5): Buffered 2V Reference Capable of 0.5mA Drive. Bypass with at least 1µF capacitor to ground.

IVINN (Pin 6): IVINN is the inverting input of the input current sense amplifier. This pin connects to the drain of the high side N-channel power FET and the input current sense resistor.

IVINP (Pin 7): IVINP is the noninverting input of the input current sense amplifier. This pin connects to the input supply V_{IN} and the input current sense resistor.

IVINMON (Pin 8): IVINMON is the buffered output of the input current sense amplifier. This pin enables monitoring of the averaged supply current with an output voltage of $20 \bullet (V_{IVINP} – V_{IVINN})$. The capacitive loading to this pin should be less than 1nF.

$\overline{FAULT}$ (Pin 9): Output Voltage Fault Detection Pin for Shorted or Open LEDs. Internal comparators pull down this pin when the FB pin voltage is lower than 0.25V or higher than 1.16V and when the inductor current is less than ten percent of the maximum value. This pin should be pulled up to $INTV_{CC}$ with a resistance higher than 10k.

FBIN (Pin 10): The FBIN pin enables peak power tracking for solar powered chargers and other similar applications by controlling the output current of the system based on the input voltage. This pin should be tied to V_{REF} if this feature is not used.

FB (Pin 11): The feedback pin is used for voltage regulation and overvoltage protection. The feedback voltage is regulated to 1.206V. When the feedback voltage exceeds 1.515V, the overvoltage lockout prevents switching.

PIN FUNCTIONS

GND (Pin 12, Pin 23, Pin 28, Exposed Pad Pin 29): Ground. The exposed pad must be soldered to the PCB.

CTRL2 (Pin 13): Thermal Control Input to Reduce the Regulated Output Current.

CTRL1 (Pin 14): The CTRL1 pin sets the regulated output current. The maximum control voltage is 1.5V. Above 1.5V, there is no change in the regulated current.

SS (Pin 15): The Soft-Start Pin. Place an external capacitor to ground to limit the regulated current during start-up conditions. The soft-start pin has an 11µA charging current. When the voltage at this pin is lower than voltages at CTRL1 and CTRL2, it overrides both signals and determines the regulated current.

SENSE$^-$ (Pin 16): SENSE$^-$ is the noninverting input of the error amplifier for the current regulation loop. The reference current, based on CTRL1, CTRL2, SS or FBIN determines the regulated voltage between SENSE$^+$ and SENSE$^-$.

SENSE$^+$ (Pin 17): SENSE$^+$ is the inverting input of the error amplifier for the current regulation loop. This pin is connected to an external current sense resistor. The voltage drop between SENSE$^+$ and SENSE$^-$ is measured against the voltage drop across an internal resistor at the input to the current regulation loop.

V_C (Pin 18): A resistor and capacitor connected in series to the V_C pin provide the necessary compensation for the stability of the average current loop. Typical values are 5k to 60k for the resistor and 2.2nF to 10nF for the capacitor.

ISMON (Pin 19): ISMON is the buffered output of the output current sense amplifier. This voltage output enables monitoring the averaged output current of the LED driver with a voltage of $20 \bullet (V_{SENSE}^+ - V_{SENSE}^-)$. The capacitive loading to this pin should be less than 1nF.

RT (Pin 20): A resistor from the RT pin to ground sets the switching frequency between 200kHz and 1MHz. When using the SYNC function, set the frequency to be at least 20% lower than the SYNC pulse frequency. This pin is current-limited to 55µA. Do not leave this pin open.

SYNC (Pin 21): Frequency Synchronization Pin. This pin allows the switching frequency to be synchronized to an external clock. The RT resistor should be chosen to operate the internal clock at 20% slower than the SYNC pulse frequency. This pin should be grounded when not in use.

PWM (Pin 22): The input pin for PWM dimming of LEDs. When low, all switching is terminated and the PWM_OUT pin is low. This pin should be connected to $INTV_{CC}$ when not in use.

PWM_OUT (Pin 24): This pin can drive an external FET for PWM dimming of LEDs. The pull-up and pull-down impedances of the driver are 2.2Ω and 0.9Ω, respectively. Do not force any voltage on this pin.

TG (Pin 25): TG is the top FET gate drive pin that controls the state of the external high side power FET. The driver pull-up impedance is 2.2Ω, and pull-down impedance is 1.3Ω. Do not force any voltage on this pin.

SW (Pin 26): The SW pin is used internally as the lower rail for the floating top FET gate driver. Externally, this node connects the two power FETs and the inductor.

BOOST (Pin 27): The BOOST pin provides a floating 5V regulated supply for the top FET gate driver. An external schottky diode is required from the $INTV_{CC}$ pin to the BOOST pin to charge the BOOST capacitor when the SW pin is near ground.

BLOCK DIAGRAM

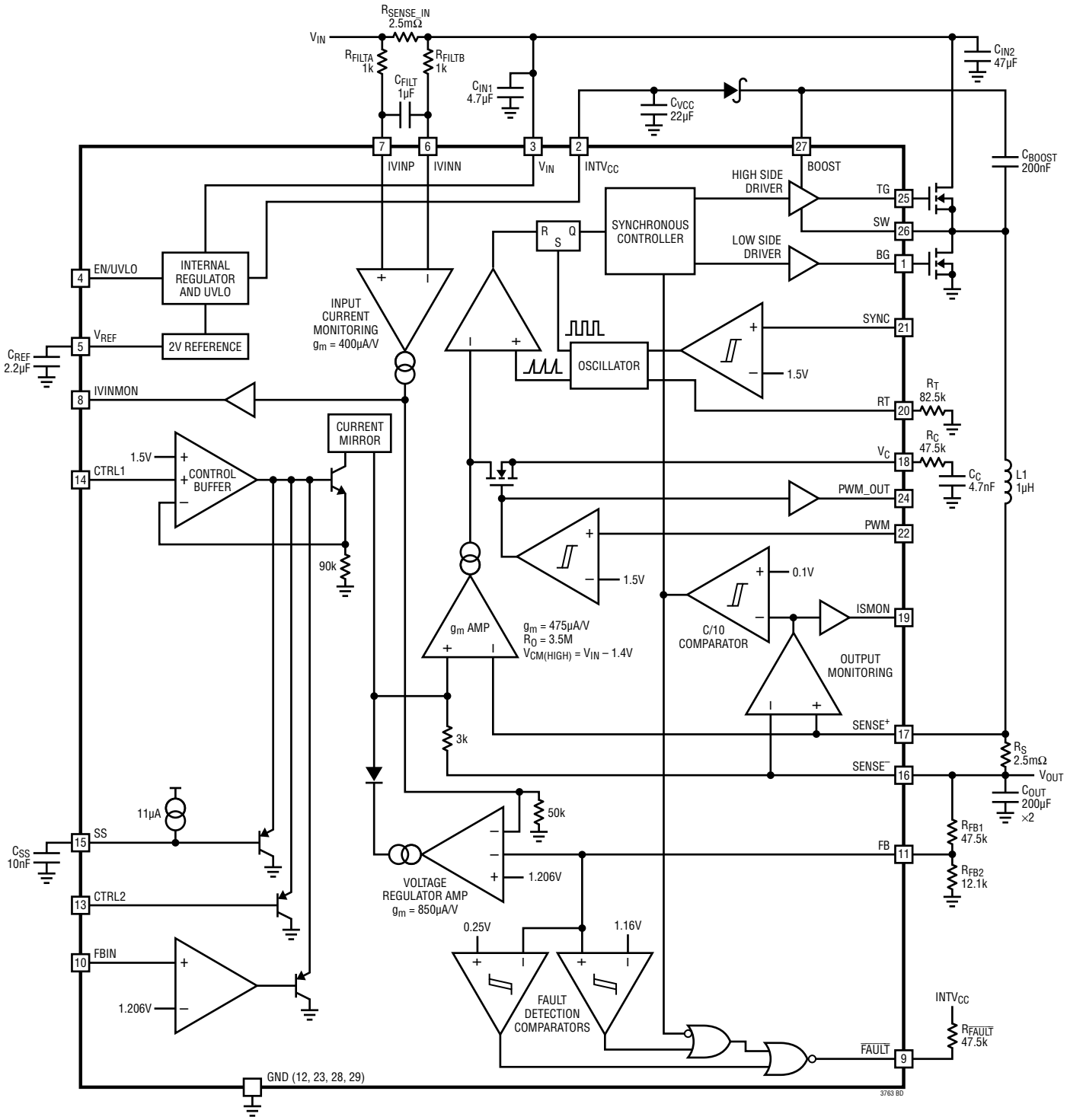


Figure 1. Block Diagram

OPERATION

The LT3763 utilizes fixed frequency, average current mode control to accurately regulate the inductor current independently from the output voltage. This is an ideal solution for applications requiring a regulated current source. The control loop will regulate the current in the inductor at an accuracy of ±6%. If the output reaches the regulation voltage determined by the resistor divider from the output to the FB pin, the inductor current will be reduced by the voltage regulation loop. In voltage regulation, the output voltage has an accuracy of ±1.5%. For additional operation information, refer to the Block Diagram in Figure 1.

The current control loop has two main inputs, determined by the voltages at the analog control pins, CTRL1 and CTRL2. The lower voltage between CTRL1 and CTRL2 determines the regulated output current. The voltages at CTRL1 and CTRL2 are buffered to produce a reference current set by the voltage across an internal 90k resistor. This reference current produces a reference voltage that the average current mode control loop uses to regulate the inductor current as a voltage drop across the external sense resistor, R_S. The outputs of the internal buffers are clamped at 1.5V, limiting the control range of the CTRL1 and CTRL2 pins from 0V to 1.5V—corresponding to a 0mV to 51mV range on R_S.

The FBIN pin provides a third input to the current control loop. This input is dedicated to regulating the input voltage by controlling the inductor current. Inductor current regulation commences when the voltage at the FBIN pin rises higher than 1.206V. Above 1.206V, the inductor current is linearly increased, providing the maximum current, as determined by the voltages at the CTRL pins, when FBIN is at and above 1.26V. When input voltage regulation is not needed, FBIN should be tied to V_{REF} to allow the CTRL pins to control the inductor current.

The 2V reference provided on the V_{REF} pin allows the use of a resistor voltage divider to the CTRL1 and CTRL2 pins. The current supplied by the V_{REF} pin should be less than 0.5mA.

The error amplifier for the average current mode control loop has a common mode lockout that regulates the inductor current so that the error amplifier is never operated out of the common mode range. The common mode range is from ground to 1.4V below the V_{IN} supply rail.

The LT3763 prevents excessive inductor current by triggering overcurrent limit when the inductor current produces a voltage greater than 85mV across the $SENSE^+$ and $SENSE^-$ pins. The current is limited on a cycle-by-cycle basis; switching shuts down as soon as the overcurrent level is reached. Overcurrent is not soft-started.

The regulated output voltage is set with a resistor divider from the output to the FB pin. The reference for the FB pin is 1.206V. If the output voltage level is high enough to engage the voltage loop, the regulated inductor current will be reduced. If the voltage at the FB pin reaches 1.515V, an internal overvoltage flag is set, shutting down switching for a brief period.

The EN/UVLO pin functions as a precision shutdown pin. When the voltage at the EN/UVLO pin is lower than 1.52V, the internal reset flag is asserted and switching is terminated. Full shutdown is guaranteed below 0.5V with a quiescent current of less than 2µA. The EN/UVLO pin has 185mV of hysteresis built in, and a 5µA current source is connected to this pin that allows any amount of hysteresis to be added with a series resistor or resistor divider from V_{IN}. Alternatively, this pin can be tied directly to V_{IN} to reduce the number of off-chip components.

During start-up, the SS pin is held low until the internal reset goes low and PWM goes high the first time after a reset event. Once the reset is cleared, the capacitor connected to the soft-start pin is charged with an 11µA current source. Initially, the internal buffers for the CTRL1, CTRL2, and FBIN voltages are limited by the voltage at the soft-start pin, and the inductor current reference slowly increases to the level determined by the lowest voltage of those three pins.

The rising threshold for thermal shutdown is set at 165°C with –5°C hysteresis. During thermal shutdown, all switching is terminated, and the part is in reset mode (forcing the SS pin low).

The switching frequency is determined by a resistor at the RT pin. This pin is limited to 55µA, which limits the switching frequency to approximately 2MHz when the RT pin is shorted to ground. The LT3763 may also be synchronized to an external clock through the use of the

OPERATION

SYNC pin which has precise thresholds at 2.175V and 1.5V for rising and falling edges, respectively.

LT3763 also features a PWM driver for LED dimming. PWM_OUT is high when the PWM pin voltage is higher than 2.175V, and low when PWM is lower than 1.5V. Switching is terminated when PWM is lower than 1.5V. PWM should be tied to $INTV_{CC}$ when the PWM function is not needed.

The $\overline{FAULT}$ pin is pulled down to ground when the voltage at FB becomes less than 0.25V which indicates a short-circuit condition. It is also pulled down to indicate an open-circuit condition when the voltage becomes greater than 1.16V and the inductor current is less than ten percent of the maximum (C/10), or equivalently, when the voltage between $SENSE^+$ and $SENSE^-$ is less than 5mV. To avoid jitter when recovering from a fault condition, 50mV hysteresis is employed in the comparators. Additionally, when the inductor current is lower than C/10, the C/10 comparator disables the low side MOSFET regardless of the voltage at FB.

The integrated input current and output current monitoring functions of the LT3763 allow users to acquire system information such as the input power and output power. The outputs of the current monitors, IVINMON and ISMON, range from 0V to 1V when the inputs vary from 0V to 50mV. When using 2.5mΩ sense resistors, for example, these current monitoring amplifiers sense from 0A to 20A. To filter out the switching portion of the currents and measure the average current information, the input pins of the input current monitor, IVINP and IVINN, should connect to the sense resistor through two 1k resistors and a capacitor directly between the IVINP and IVINN pins. The capacitance value can be adjusted according to the switching frequency and the ripple magnitude. The output current monitor employs an internal filter to reduce ripple, and it does not require an external filter, but if one is added, the corner frequency should be higher than the switching frequency.

The LT3763 also includes an input current limiting function to regulate the input current to a value determined by the R_{SENSE_IN} resistor. When the voltage drop across the R_{SENSE_IN} resistor approaches 50mV, the inductor current is reduced and regulated so that 50mV is maintained across the IVINP and IVINN pins.

APPLICATIONS INFORMATION

Programming Inductor Current

The analog voltage at the CTRL1 pin is buffered and produces a reference voltage, V_{CTRL}, across an internal resistor. The regulated average inductor current is determined by:

$$I_O = \frac{V_{CTRL}}{30 \bullet R_S}$$

where R_S is the external sense resistor and I_O is the average inductor current, which is equal to the output current. Figure 2 shows the maximum output current versus R_S. The maximum power dissipation in the resistor will be:

$$P_{RS} = \frac{(0.05V)^2}{R_S}$$

Figure 3 plots the power dissipation in R_S, and Table 1 lists several resistance values and the corresponding maximum inductor current and sense-resistor power dissipation. Susumu, Panasonic and Vishay offer accurate sense resistors.

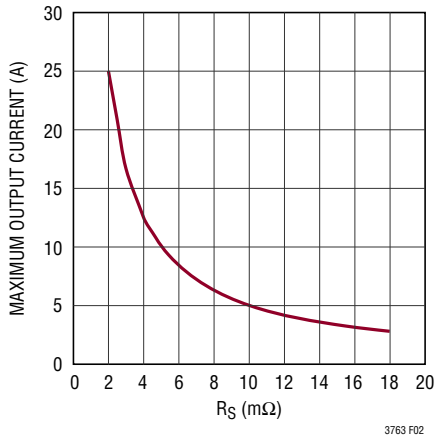


Figure 2. R_S Value Selection for Regulated Output Current

APPLICATIONS INFORMATION

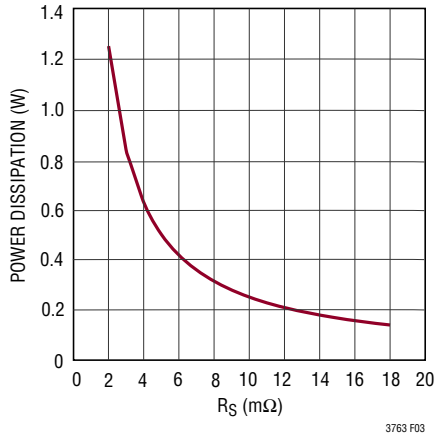


Figure 3. Power Dissipation in R_S

Table 1. Sense Resistor Values

MAXIMUM OUTPUT CURRENT (A)	RESISTOR, R_S (mΩ)	POWER DISSIPATION (W)
1	50	0.05
5	10	0.25
10	5	0.50
25	2	1.25

Inductor Selection

Size the inductor so that the peak-to-peak ripple current is approximately 30% of the output current.

The following equation sizes the inductor for best performance:

$$L = \left(\frac{V_{IN} \bullet V_O - V_O^{\,2}}{0.3 \bullet f_{SW} \bullet I_O \bullet V_{IN}} \right)$$

where V_O is the output voltage, V_{IN} is the input voltage, I_O is the maximum regulated current in the inductor and f_{SW} is the switching frequency.

The overcurrent comparator terminates switching when the voltage between the $SENSE^+$ and $SENSE^-$ pins exceeds 85mV. The saturation current for the inductor should be at least 20% higher than the maximum regulated current. Recommended inductor manufacturers are listed in Table 2.

Table 2. Recommended Inductor Manufacturers

VENDOR	WEBSITE
Coilcraft	www.coilcraft.com
Sumida	www.sumida.com
Vishay	www.vishay.com
Würth Electronics	www.we-online.com
NEC-Tokin	www.nec-tokin.com

Switching MOSFET Selection

The following parameters are critical in determining the best switching MOSFETs for a given application: total gate charge (Q_G), on-resistance ($R_{DS(ON)}$), gate to drain charge (Q_{GD}), gate-to-source charge (Q_{GS}), gate resistance (R_G), breakdown voltages (maximum V_{GS} and V_{DS}) and drain current (maximum I_D). The following guidelines provide information to make the selection process easier, and Table 3 lists some recommended parts and manufacturers.

For both switching MOSFETs the rated drain current should be greater than the maximum inductor current. Use the following equation to calculate the peak inductor current:

$$I_{MAX} = I_O + \left(\frac{V_{IN} \bullet V_O - V_O^{\,2}}{2 \bullet f_{SW} \bullet L \bullet V_{IN}} \right)$$

The rated drain current is temperature dependent, and most data sheets include a table or graph of the rated drain current versus temperature.

The rated V_{DS} should be higher than the maximum input voltage (including transients) for both MOSFETs. As for the rated V_{GS}, the signals driving the gates of the switching MOSFETs have a maximum voltage of 5V with respect to the source. However, during start-up and recovery conditions, the gate-drive signals may be as low as 3V. Therefore, to ensure that the LT3763 recovers properly, the maximum threshold voltage should be less than 2V, and for a robust design, ensure that the rated V_{GS} is greater than 7V.

Power losses in the switching MOSFETs are related to the on-resistance, $R_{DS(ON)}$; gate resistance, R_G; gate-to-drain charge, Q_{GD} and gate-to-source charge, Q_{GS}. Power lost to the on-resistance is an Ohmic loss, $I^2R_{DS(ON)}$, and usually dominates for input voltages less than 15V. Power lost while charging the gate capacitance dominates for voltages

APPLICATIONS INFORMATION

greater than 15V. When operating at higher input voltages, efficiency can be optimized by selecting a high side MOSFET with higher $R_{DS(ON)}$ and lower Q_G. The total power loss in the high side MOSFET can be approximated by:

P_{LOSS} = ohmic loss + transition loss

$$P_{LOSS} \approx \left(\frac{V_O}{V_{IN}} \bullet I_O{}^2 R_{DS(ON)} \bullet \rho_T\right) + \left(\left(\frac{V_{IN} \bullet I_{OUT}}{5V}\right) \bullet \left(\frac{(Q_{GD} + Q_{GS}) \bullet}{(2 \bullet R_G + R_{PU} + R_{PD})}\right) \bullet f_{SW}\right)$$

where ρ_T is a dimensionless temperature dependent factor in the MOSFET's on-resistance. Using 70°C as the maximum ambient operating temperature, ρ_T is roughly equal to 1.3. R_{PD} and R_{PU} are the LT3763 high side gate driver output impedances: 1.3Ω and 2.2Ω, respectively.

A good approach to MOSFET sizing is to select a high side MOSFET, then select the low side MOSFET. The trade-off between $R_{DS(ON)}$, Q_G, and Q_{GS} for the high side MOSFET is evident in the following example. V_O is equal to 4V. These two N-channel MOSFETs are rated for a V_{DS} of 40V and mounted in the same package, but with 8× different $R_{DS(ON)}$ and 4.5× different Q_G and Q_{GD}:

M1: $R_{DS(ON)}$ = 2.3mΩ, Q_G = 45.5nC,

Q_{GS} = 13.8nC, Q_{GD} = 14.4nC, R_G = 1Ω

M2: $R_{DS(ON)}$ = 18mΩ, Q_G = 10nC,

Q_{GS} = 4.5nC, Q_{GD} = 3.1nC, R_G = 3.5Ω

Power loss for both MOSFETs is shown in Figure 4. Observe that whereas the $R_{DS(ON)}$ of M1 is eight times lower, the power loss at low input voltages is about equal to that of M2, and at high voltages, it is four times higher.

Power loss within the low side MOSFET is almost entirely from the $R_{DS(ON)}$ of the FET. Select the low side FET with the lowest $R_{DS(ON)}$ while keeping the total gate charge Q_G to 30nC or less.

Another power loss related to switching MOSFET selection is the power lost driving the gates. The total gate charge, Q_G, must be charged and discharged each switching cycle, so the power lost to the charging of the gates is:

$P_{GATE} = V_{IN} \bullet (Q_{GLG} + Q_{GHG}) \bullet f_{SW}$

where Q_{GLG} is the low side gate charge and Q_{GHG} is the high side gate charge.

The majority of this loss occurs in the internal LDO within the LT3763:

$P_{LOSS\_LDO} \approx (V_{IN} - 5V) \bullet (Q_{GLG} + Q_{GHG}) \bullet f_{SW}$

Whenever possible, utilize a switching MOSFET that minimizes the total gate charge to limit the internal power dissipation of the LT3763. Some recommended MOSFETs are listed in Table 3.

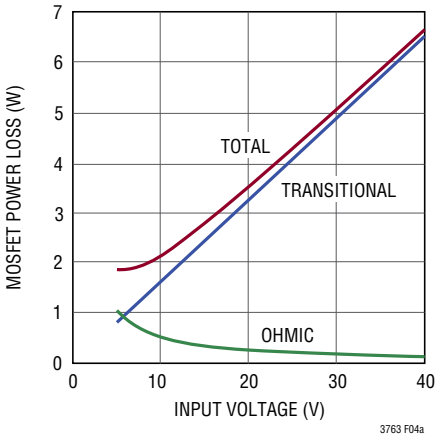


Figure 4a. Power Loss Example for M1

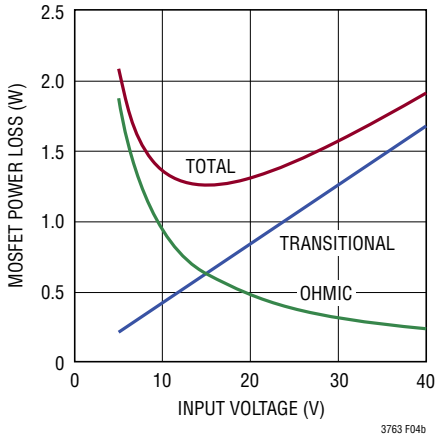


Figure 4b. Power Loss Example for M2

APPLICATIONS INFORMATION

Table 3. Recommended Switching FETs

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	TOP FET	BOTTOM FET	MANUFACTURER
60	4	20	RJK0853DPB	RJK0853DPB	Renesas www.renesas.com
24	4	5	RJK0368DPA	RJK0332DPB	
48	10 to 35	10	RJK0851DPB	RJK0851DPB	
12	2 to 4	10	FDMS8680	FDMS8672AS	Fairchild www.fairchildsemi.com
26	4	20	Si7884BDP	SiR470DP	Vishay www.vishay.com
24	4	40	PSMN4R0-30YL	RJK0346DPA	NXP/Philips www.nxp.com
36	12	10	BSC100N06LS3	BSC100N06LS3	www.infineon.com

Input Capacitor Selection

The input capacitor should be sized at least 2µF for every 1A of output current and placed very close to the high side MOSFET. The loop created by the input capacitor, high side MOSFET, low side MOSFET should be minimized. It should have a ripple current rating equal to half of the maximum output current. Additionally, a small 4.7µF ceramic capacitor should be placed between V_{IN} and ground as close as possible to the V_{IN} pin and the exposed pad of the package for optimal noise immunity.

It is recommended that several low ESR (equivalent series resistance) ceramic capacitors be used as the input capacitance, although other capacitors with higher density may be required to reduce board area. Only X5R or X7R capacitors maintain their capacitance over a wide range of operating voltages and temperatures.

Output Capacitor Selection

The output capacitors need to have very low ESR to reduce output ripple. A minimum of 20µF/A of load current should be used in most designs. The capacitors also need to be surge rated to the maximum output current. To achieve the lowest possible ESR, several low ESR ceramic capacitors should be used in parallel. Many lower output voltage applications benefit from the use of high density POSCAP capacitors, which are easily destroyed when exposed to overvoltage conditions. To prevent this, select POSCAP capacitors that have a voltage rating that is at least 50% higher than the regulated voltage.

Note that when dimming, the output voltage increases at the end of every pulse as the decreasing inductor current flows into the output capacitor. Use of a small output capacitor may trigger overvoltage protection through the FB pin.

C_{BOOST} Capacitor Selection

The C_{BOOST} capacitor must be sized no bigger than 220nF and more than 50nF to ensure proper operation of the LT3763. Use 220nF for high current switching MOSFETs with high gate charge.

$INTV_{CC}$ Capacitor Selection

The bypass capacitor for the $INTV_{CC}$ pin should be larger than 22µF to ensure stability, and it should be connected as close as possible to the exposed pad underneath the package. It is recommended that the ESR be lower than 50mΩ to reduce noise within the LT3763. For driving MOSFETs with gate charges larger than 44nC, use 0.5µF/nC of total gate charge.

Soft-Start

Unlike conventional voltage regulators, the LT3763 utilizes the soft-start function to control the regulated inductor current instead of the output voltage. The charging current is 11µA and reduces the set current as long as the SS pin voltage is lower than CTRL1 and CTRL2.

Output Current Regulation

To adjust the regulated load current, an analog voltage is applied to the CTRL1 pin. Figure 5 shows the regulated voltage across the sense resistor for control voltages up to

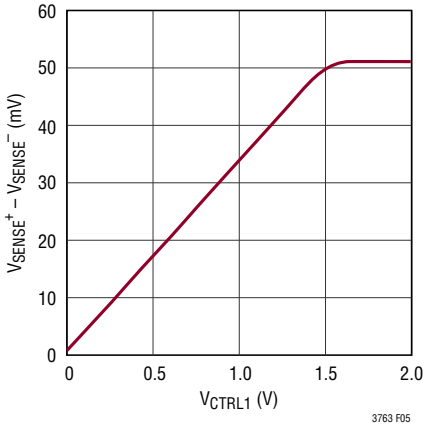


Figure 5. Sense Voltage vs CTRL Voltage

APPLICATIONS INFORMATION

2V. Figure 6 shows the CTRL1 voltage created by a voltage divider from V_{REF} to ground. When sizing the resistor divider, please be aware that the V_{REF} pin should have a total load current less than 0.5mA, and that above 1.5V, the control voltage has no effect on the regulated inductor current. Setting CTRL1 to 0V does not automatically stop switching. To disable switching, set PWM pin voltage below 1.5V.

Input Current Monitoring

Users can monitor the input current at the IVINMON pin, which produces 0V to 1V as the voltage between IVINP and IVINN varies from 0mV to 50mV, as shown in Figure 7. Due to the switching of the high side FET, the input current is noisy and monitoring the average input current requires an external filter with 1k resistors connecting IVINP and IVINN to the input current sense resistor R_{SENSE_IN}. Choose the capacitor for this filter according to the switching frequency so that the noise is reduced by at least a factor of 100. If the frequency is 500kHz, for example, 1µF is sufficient, and higher switching frequencies will require a smaller capacitor. A resistor and capacitor may be connected to IVINMON to further filter the noise. With both input and output current monitoring, the LT3763 enables users to calculate the overall efficiency of the circuit including the losses in the external components.

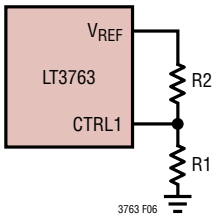


Figure 6. Analog Control of Inductor Current

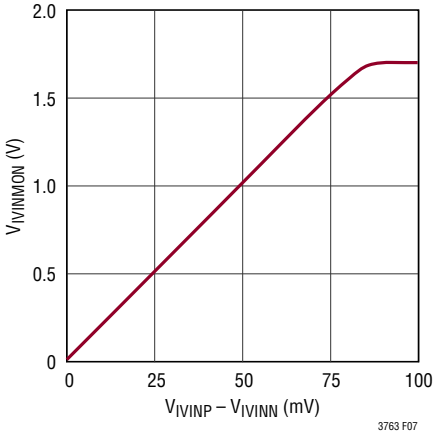


Figure 7. Input Current Monitoring Voltage vs Input Current Sense Voltage

Output Current Monitoring

The LT3763 provides users the capability to monitor the output current as a voltage provided at the ISMON pin. The voltage will linearly increase from 0V to 1V as the voltage between $SENSE^+$ and $SENSE^-$ increases from 0mV to 50mV as shown in Figure 8. If, for example, a 2.5mΩ resistor is chosen for R_S, then a 1V output at ISMON will indicate a 20A output current. A resistor and capacitor may be connected to ISMON to filter noise.

Voltage Regulation and Overvoltage Protection

The LT3763 uses the FB pin to regulate the output voltage and to provide an overvoltage lockout to avoid high voltage conditions. The regulated output voltage is programmed using a resistor divider from the output to the FB pin (Figure 9). When the output voltage approaches

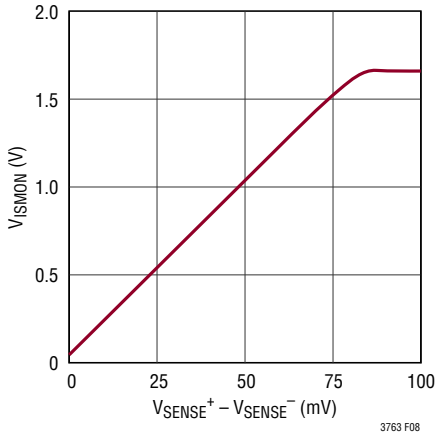


Figure 8. Output Current Monitoring Voltage vs Output Current Sense Voltage

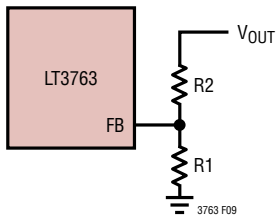


Figure 9. Output Voltage Regulation and Overvoltage Protection Feedback Connections

APPLICATIONS INFORMATION

the programmed level (1.206V at the FB pin), the voltage error amplifier overrides CTRL1 to set the inductor current and regulate V_{OUT}. When the output voltage exceeds 125% of the regulated voltage level (1.515V at the FB pin), the internal overvoltage flag is set, terminating switching. The regulated output voltage must be greater than 1.5V and is set by the equation:

$$V_{OUT} = 1.206V\left(1+\frac{R2}{R1}\right)$$

Fault Detection

The LT3763 detects that the load has had an open-circuit or short-circuit event indicated by pulling the $\overline{FAULT}$ pin to ground. These conditions are detected by comparing the voltage at the FB pin to two internal reference voltages. A short-circuit is defined as V_{FB} lower than 0.25V. In an open-circuit condition, the regulated inductor current will charge the output capacitor, the voltage at FB will begin to increase, and the voltage error amplifier will begin to reduce the inductor current. The open-circuit condition will be indicated at $\overline{FAULT}$ when FB is higher than 1.16V and the inductor current is less than ten percent (C/10) of the maximum value set by the sense resistor R_S. The output voltage will be regulated as determined by the resistor divider to the FB pin.

Low Current Detection

When the inductor current decreases to ten percent of the maximum current, the C/10 comparator will also disable the low side gate driver, so the converter will become non-synchronous and automatically transition into discontinuous conduction mode when the inductor current is low enough relative to the ripple.

The low current condition is an essential part of battery charging applications. The LT3763 works well in this application delivering a constant current to the battery as it charges and then automatically reducing the current to a trickle charge as the battery voltage approaches its fully charged value. In this application, the signal at $\overline{FAULT}$ triggered by the low current detection comparator serves as an indicator that the trickle charge phase of charging the battery has begun.

Programming Switching Frequency

The LT3763 has an operational switching frequency range between 200kHz and 1MHz. This frequency is programmed with an external resistor from the RT pin to ground. Do not leave this pin open under any condition. The RT pin is also current-limited to 55µA. See Table 4 and Figure 10 for resistor values and the corresponding switching frequencies.

Table 4. Switching Frequency

SWITCHING FREQUENCY (MHz)	R_T (kΩ)
1.00	40.2
0.75	53.6
0.50	82.5
0.30	143
0.20	221

Switching Frequency Synchronization

The nominal switching frequency of the LT3763 is determined by the resistor from the RT pin to ground and may be set from 200kHz to 1MHz. The internal oscillator may also be synchronized to an external clock through the SYNC pin. The external clock applied to the SYNC pin must have a logic low below 1.5V and a logic high above 2.175V. The input frequency must be 20% higher than the frequency that would otherwise be determined by the resistor at the RT pin. Input signals outside of these specified parameters will cause erratic switching behavior and subharmonic oscillations. Synchronization is tested at 500kHz with a 221k R_T resistor. Operation under other conditions is guaranteed by design. When synchronizing to an external

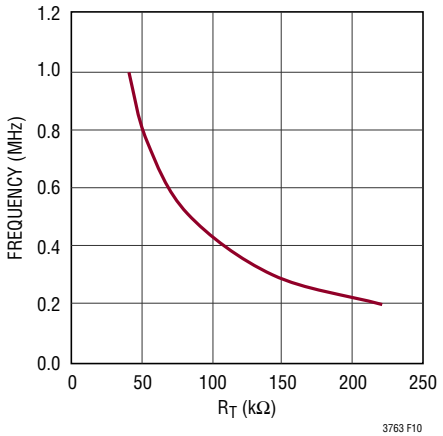


Figure 10. Frequency vs R_T Resistance

APPLICATIONS INFORMATION

clock, please be aware that there will be a fixed delay from the input clock edge to the edge of the signal at the SW pin. The SYNC pin must be grounded if the synchronization to an external clock is not required. When SYNC is grounded, the switching frequency is determined by the resistor R_T.

PWM Driver

The LT3763 includes a PWM driver for users who want to control the dimming of LEDs connected to the output. The driver will pull up the gate of an external N-channel MOSFET connected to the PWM_OUT pin when the voltage at the PWM pin rises above 2.175V and pull down the gate when the voltage falls below 1.5V. When V_{PWM} is lower than 1.5V, switching is terminated and V_C is disconnected from the current regulation amplifier. When V_{PWM} is above 2.175V, the inductor current is regulated to the current programmed by the voltage at the CTRL1, CTRL2, or FBIN pins.

The pull-up driver impedance is 2.2Ω, and the pull-down driver impedance is 0.9Ω. The PWM dimming pulse-width should be longer than two switching cycles.

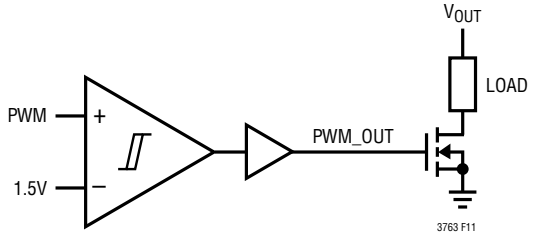


Figure 11. PWM Driver Operation

PWM Operation

When the voltage at PWM is low, all switching of the high and low side MOSFETS is terminated, and the inductor current will decrease to zero. After PWM increases above the logic threshold, the inductor current ramps up to the regulated value. The ramp time, t_D, can be estimated using the following equation:

$$t_D = \frac{L \bullet I_O}{V_{IN} - V_O}$$

which assumes that the output capacitor does not discharge significantly in the time that PWM is low.

When the PWM functionality is not desired, the PWM pin should be tied to $INTV_{CC}$ so as not to disable switching.

PWM MOSFET Selection

The rated V_{DS} for the PWM MOSFET need only be higher than the maximum output voltage. Although this permits a MOSFET choice with a smaller Q_G specification than that of the switching MOSFETs, it will have little effect on efficiency, because the PWM switching frequency will be much lower than that of the switching MOSFETs. Power lost charging the gate of the PWM MOSFET will naturally be much lower than the power lost charging the switching MOSFETs. $R_{DS(ON)}$ conduction losses in the PWM MOSFET will also be much smaller if the duty cycle of the PWM signal is very low.

Like the drivers for the switching MOSFETs, the PWM driver draws power from the $INTV_{CC}$ pin, and the choice of MOSFET should follow the same recommendations for threshold voltage (less than 2V) and rated V_{GS} (at least 7V).

Thermal Shutdown

The internal thermal shutdown within the LT3763 engages at 165°C and terminates switching and discharges the soft-start capacitor. When the part has cooled to 160°C, the internal reset is cleared and the soft-start capacitor is allowed to charge.

Shutdown and UVLO

The LT3763 has an internal UVLO that terminates switching, resets all synchronous logic, and discharges the soft-start capacitor for input voltages below 4V. The LT3763 also has a precision shutdown at 1.52V on the EN/UVLO pin. Partial shutdown occurs at 1.52V and full shutdown is guaranteed below 0.5V with less than 2µA I_Q in the full shutdown state. Below 1.52V, an internal current source provides 5µA of pull-down current to allow for programmable UVLO hysteresis. The following equations determine the voltage-divider resistors for programming the UVLO voltage and hysteresis as configured in Figure 12.

$$R2 = \frac{V_{HYST}}{5\mu A} - \frac{V_{UVLO}}{51\mu A}$$

$$R1 = \left(\frac{1.52V \bullet R2}{V_{UVLO} - 1.52V} \right)$$

APPLICATIONS INFORMATION

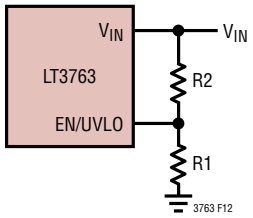


Figure 12. UVLO Configuration

Load Current Derating Using the CTRL2 Pin

The LT3763 is designed specifically for driving high power loads. In high current applications, derating the maximum current based on operating temperature prevents damage to the load. In addition, many applications have thermal limitations that will require the regulated current to be reduced based on load temperature and/or board temperature. To achieve this, the LT3763 uses the CTRL2 pin to reduce the effective regulated current in the load, which is otherwise programmed by the analog voltage at the CTRL1 pin. The load/board temperature derating is programmed using a resistor divider with a temperature dependant resistance (Figure 13). When the load/board temperature rises, the CTRL2 voltage will decrease. When the CTRL2 voltage is lower than voltage at the CTRL1 pin, the regulated current is reduced.

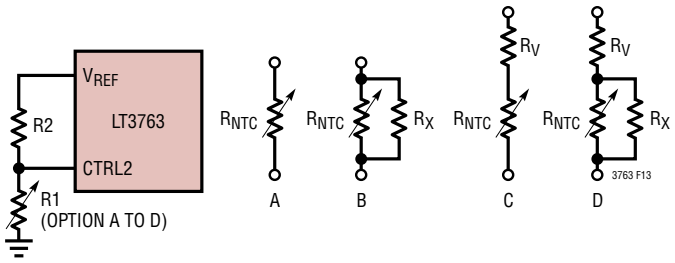


Figure 13. Load Current Derating vs Temperature Using NTC Resistor

Average Current Mode Control Compensation

The use of average current mode control allows for precise regulation of the inductor current and load current. Figure 14 shows the average current mode control loop used in the LT3763, where the regulation current is programmed by a current source and a 3k resistor.

To design the compensation network, the maximum compensation resistor needs to be calculated. In current mode controllers, the ratio of the sensed inductor current ramp

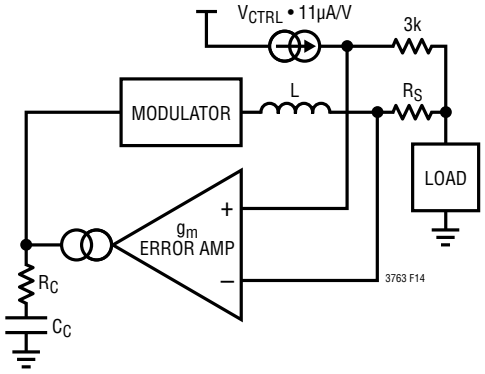


Figure 14. LT3763 Average Current Mode Control Scheme

to the slope compensation ramp determines the stability of the current regulation loop above 50% duty cycle. In the same way, average current mode controllers require the slope of the error voltage to not exceed the PWM ramp slope during the switch off time.

Since the closed loop gain at the switching frequency produces the error signal slope, the output impedance of the error amplifier will be the compensation resistor, R_C. Use the following equation as a good starting point for compensation component sizing:

$$R_C = \frac{1k\Omega \bullet 1V \bullet L}{V_O \bullet R_S \bullet T_{SW}},\ C_C = \frac{2nF}{\mu s} \bullet T_{SW}$$

APPLICATIONS INFORMATION

where T_{SW} is the switching period, L is the inductance value, V_O is the output voltage and R_S is the sense resistor. For most applications, a 4.7nF compensation capacitor is adequate and provides excellent phase margin with optimized bandwidth. Please refer to Table 5 for recommended compensation values.

Board Layout Considerations

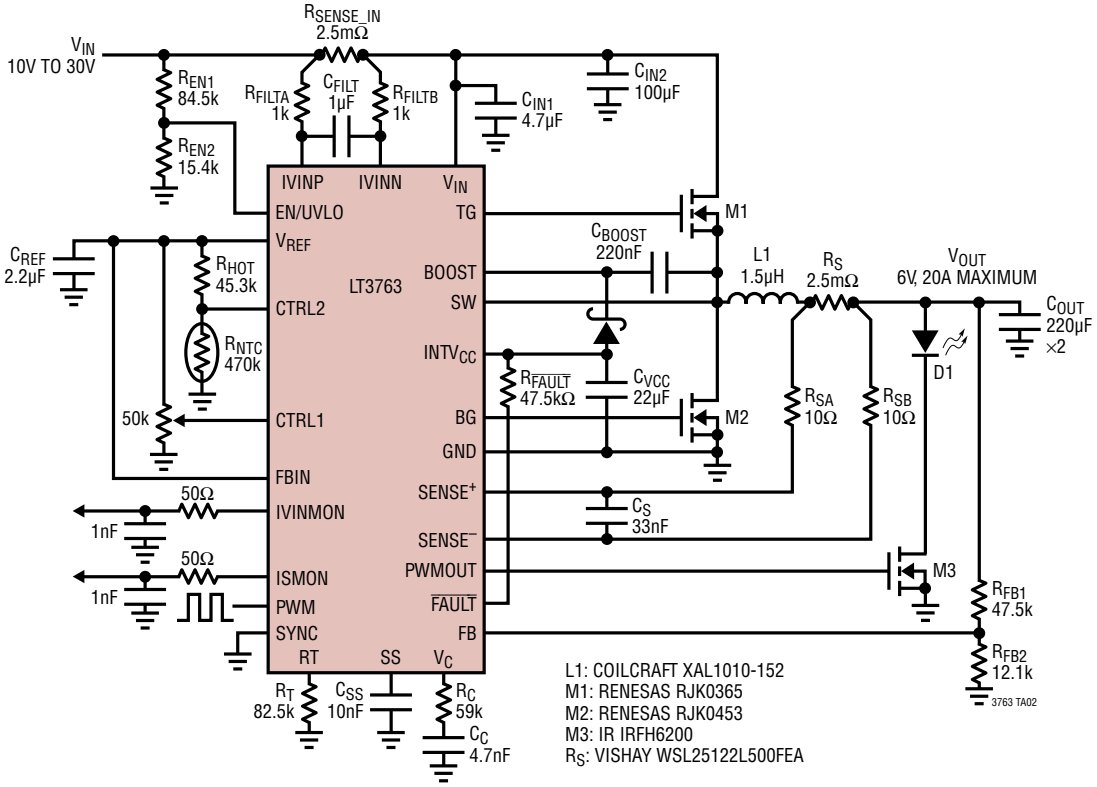
Average current mode control is relatively immune to the switching noise associated with other types of control schemes. Nevertheless, the high di/dt loop formed by input capacitors and switching MOSFETS should be minimized. Placing the sense resistor as close as possible to the $SENSE^+$ and $SENSE^-$ pins also helps avoid noise issues. Due to sense resistor ESL (equivalent series inductance), 10Ω resistors in series with the $SENSE^+$ and $SENSE^-$ pins with a 33nF capacitor placed between the SENSE pins are recommended. Utilizing a good ground plane underneath the switching components will minimize interplane noise coupling. To dissipate the heat from the switching components, use a large area for the switching node while keeping in mind that this negatively affects the radiated noise.

Table 5. Recommended Compensation Component Values (V_{CTRL2} = 2V)

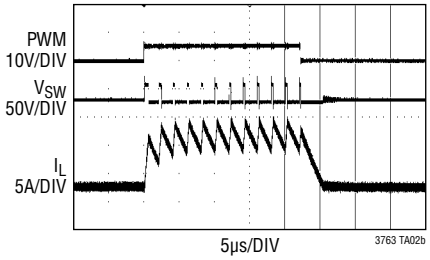
V_{IN} (V)	V_O (V)	V_{CTRL1} (V)	I_L (A)	f_{SW} (kHz)	L (µH)	R_S (mΩ)	R_C (kΩ)	C_C (nF)
12	4	0.75	5	500	2.2	5	54.9	4.7
12	4	1.50	10	500	2.2	5	54.9	4.7
12	5	1.50	20	250	2.2	2.5	44.2	8.2
60	30	0.15	1	500	10	5	15.4	4.7
60	30	1.20	8	500	10	5	15.4	4.7

TYPICAL APPLICATIONS

20A, Pulse Width Modulated, Single LED Driver

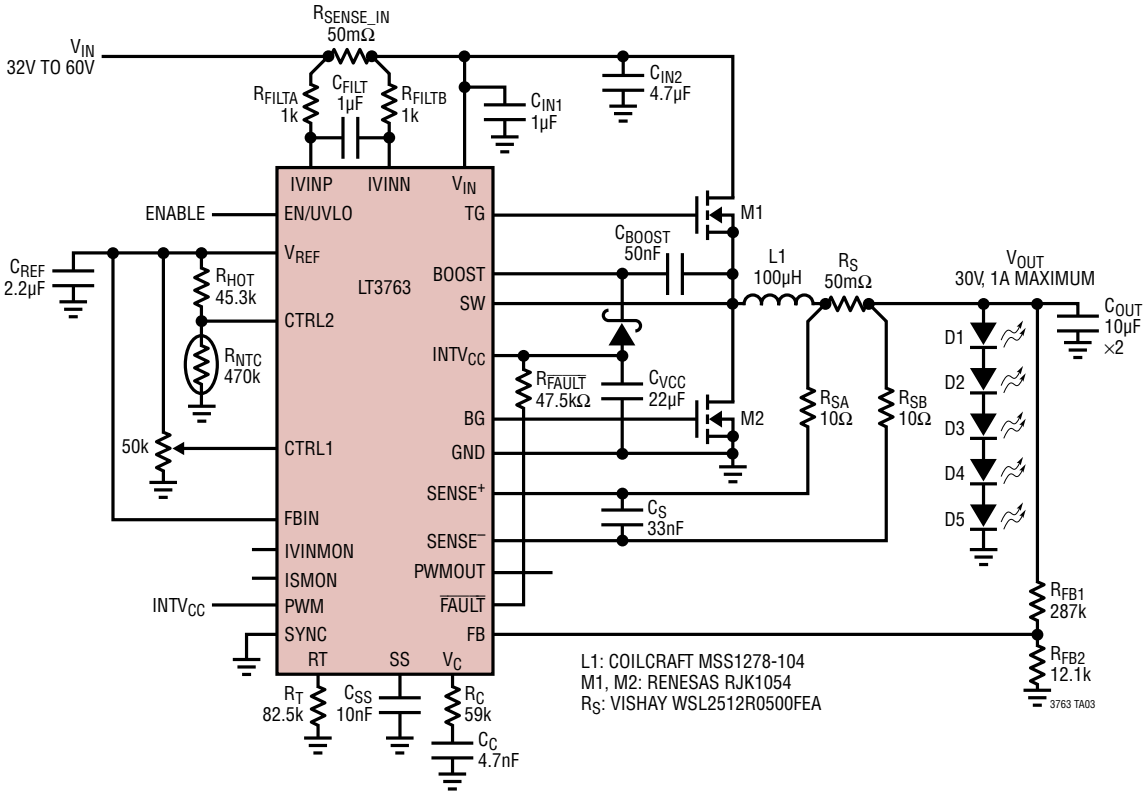


PWM Dimming



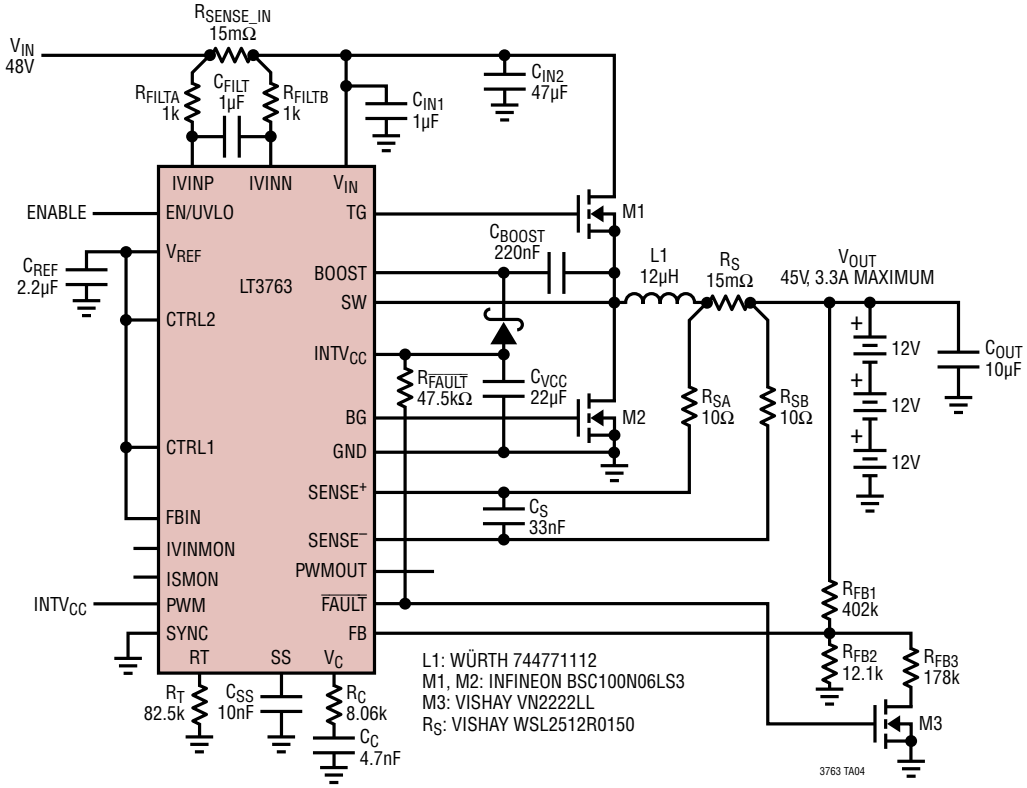
TYPICAL APPLICATIONS

1A, Five LED Driver

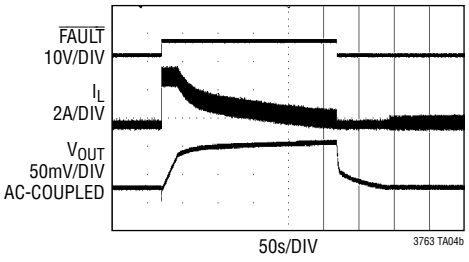


TYPICAL APPLICATIONS

3.3A, Six-Cell (36V) SLA Battery Charger

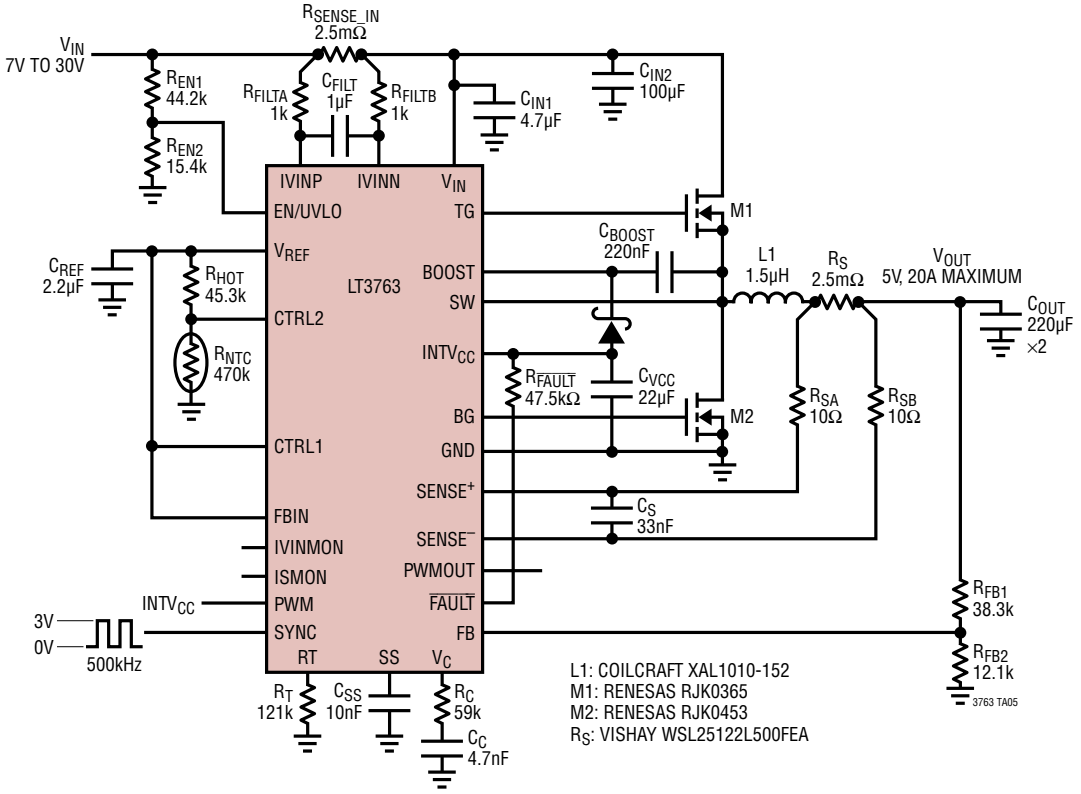


36V SLA Battery Charging

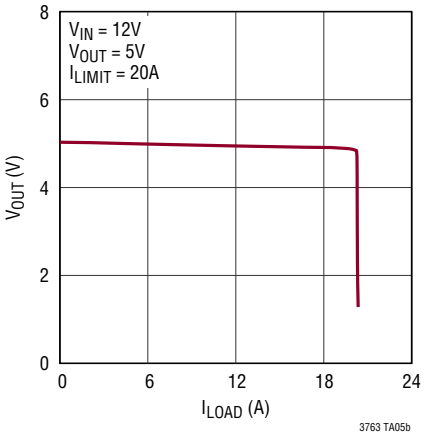


TYPICAL APPLICATIONS

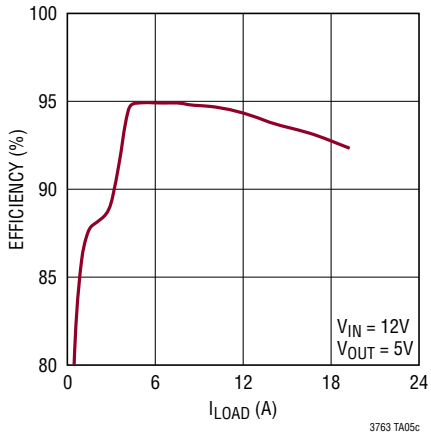
20A, Synchronized, 5V Regulator



Output Voltage Load Regulation

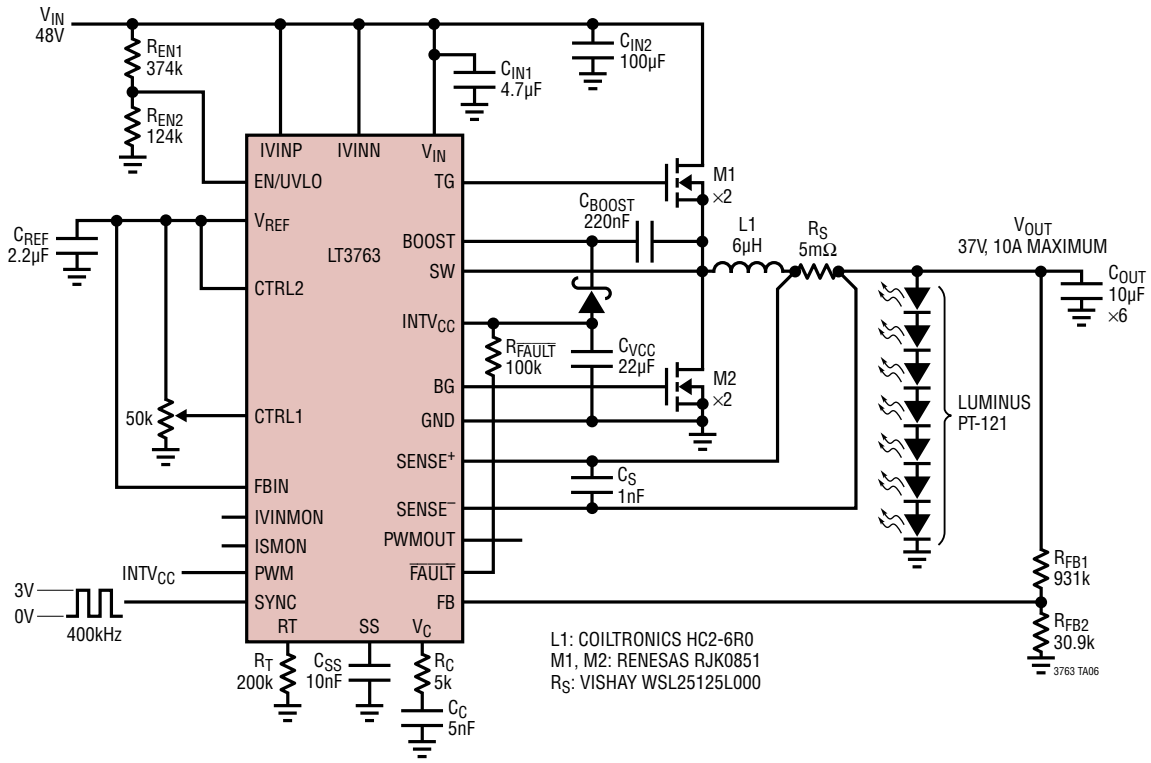


Efficiency vs Load Current

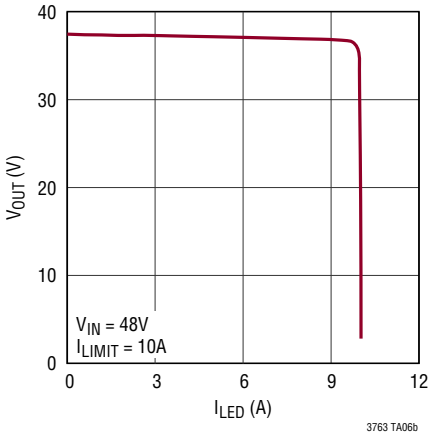


TYPICAL APPLICATIONS

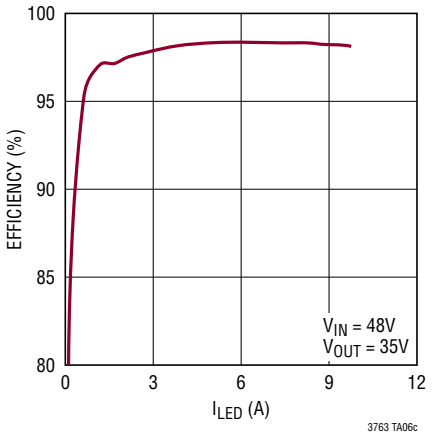
350W White LED Driver



Maximum Output Voltage

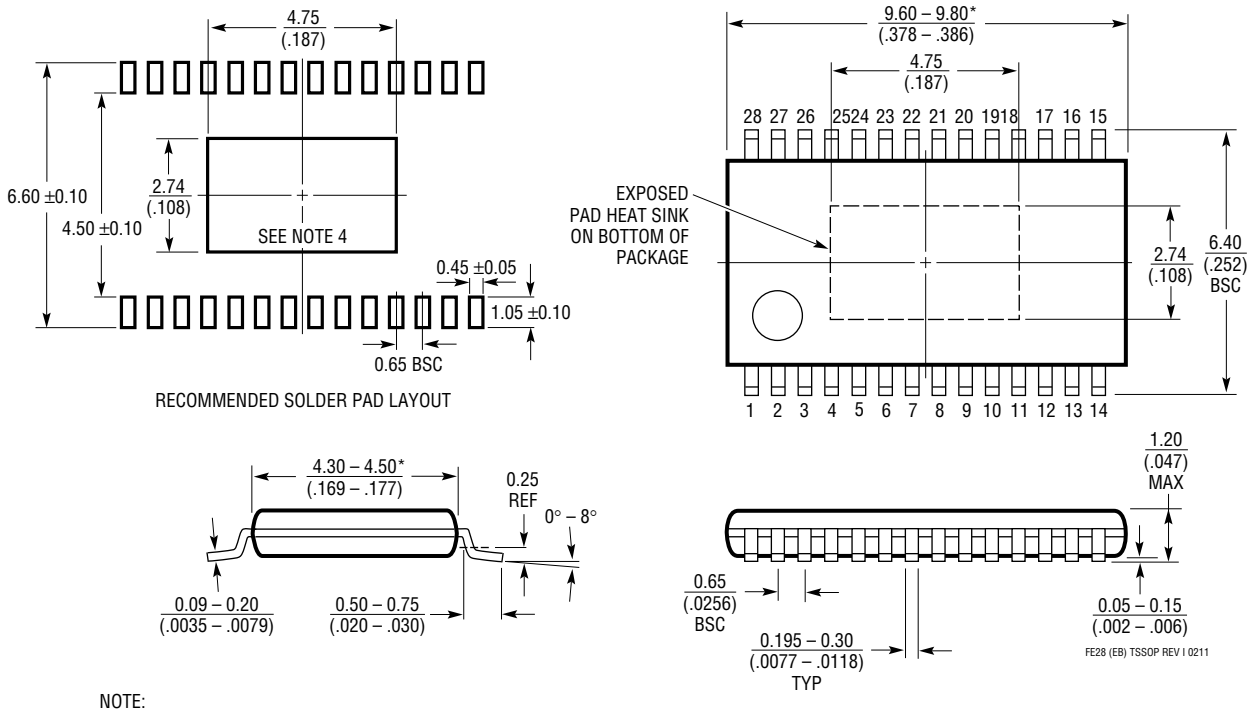


Efficiency vs LED Current



PACKAGE DESCRIPTION

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev I)
Exposed Pad Variation EB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

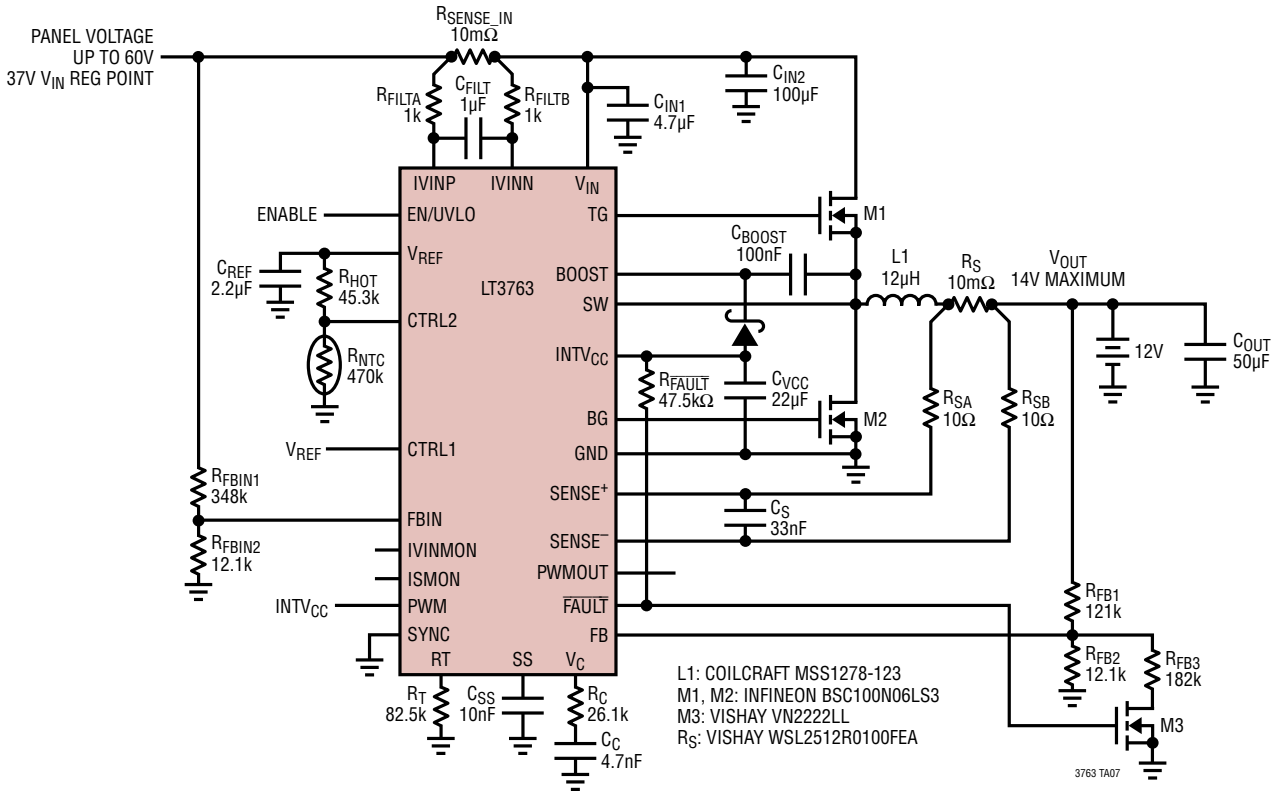
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

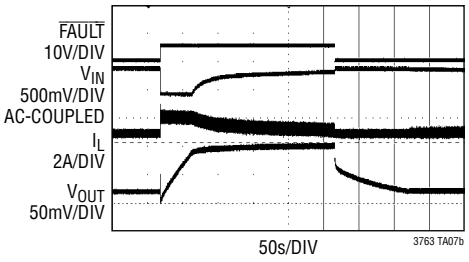
REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/13	Clarified switching frequency resistor values	3
		Clarified offset voltage conditions	4
		Clarified programming resistor value	4
		Clarified end of 7th paragraph	13
		Clarified C_{BOOST} capacitor	17
		Clarified programming resistor value and Figure 10	19
		Clarified schematic	25, 27, 30
B	10/15	Revised UVLO hysteresis equation	20
		Corrected inductor part number	25
		Clarified schematic	30
C	10/19	EC Table Fault Comparator Lower Fault Threshold (FB Falling) Specification; Max Number Changed from 0.26V to 0.265V	3
		Incorrect Table Number, Table Heading and Text Reference; Change Table 6 to Table 5	22

TYPICAL APPLICATION

70W, Solar Energy Harvester Compatible with Maximum Power Point Regulation



Solar Powered SLA Battery Charging



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3743	Synchronous Step-Down LED Driver Controller	92% Efficiency, I_{OUT} to 20A, V_{IN}: 5.5V to 36V, I_Q = 2mA, I_{SD} < 1µA, 4mm × 5mm QFN-28, TSSOP-28E
LT3741	Synchronous Step-Down LED Driver Controller	94% Efficiency, I_{OUT} to 20A, V_{IN}: 6V to 36V, I_Q = 1.8mA, I_{SD} < 1µA, 4mm × 4mm QFN-20, TSSOP-20E
LT3791	Synchronous Buck-Boost LED Driver Controller	98.5% Efficiency, I_{OUT} to 25A, V_{IN}: 4.7V to 60V, TSSOP-38E