HV6810

10-Channel Serial-Input Latched Display Driver

Features

- High Output Voltage 80V
- High-speed 5 MHz at 5 V_{DD}
- Low-power I_{BB} ≤ 0.1 mA (All High)
- Active Pull-down 100 µA Minimum at 25°C
- Output Source Current 25 mA at 60V V_{BB}
- 10-channel Display Driver
- High-speed Serially-shifted Data Input
- 5V CMOS-compatible Inputs
- Latches on all Driver Outputs
- Pin-compatible Replacement for UCN5810A, TL4810A and TL4810B

Applications

- High-speed Dot Matrix Print Head Driver
- Vacuum Fluorescent Display (VFD) Driver

General Description

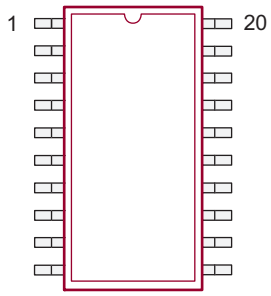
The HV6810 is a monolithic integrated circuit designed to drive a dot matrix or segmented VFD. These devices feature a serial data output to cascade additional devices for large displays.

A 10-bit data word is serially loaded into the shift register on the positive-going transition of the clock. Parallel data are transferred to the output buffers through a 10-bit D-type latch while the latch enable input is high. The data are latched when the latch enable is low. When the blanking input is high, all of the outputs are low.

Outputs are structures formed by double-diffused MOS (DMOS) transistors with output voltage ratings of 80V and 25 mA source-current capability. All inputs are compatible with CMOS levels.

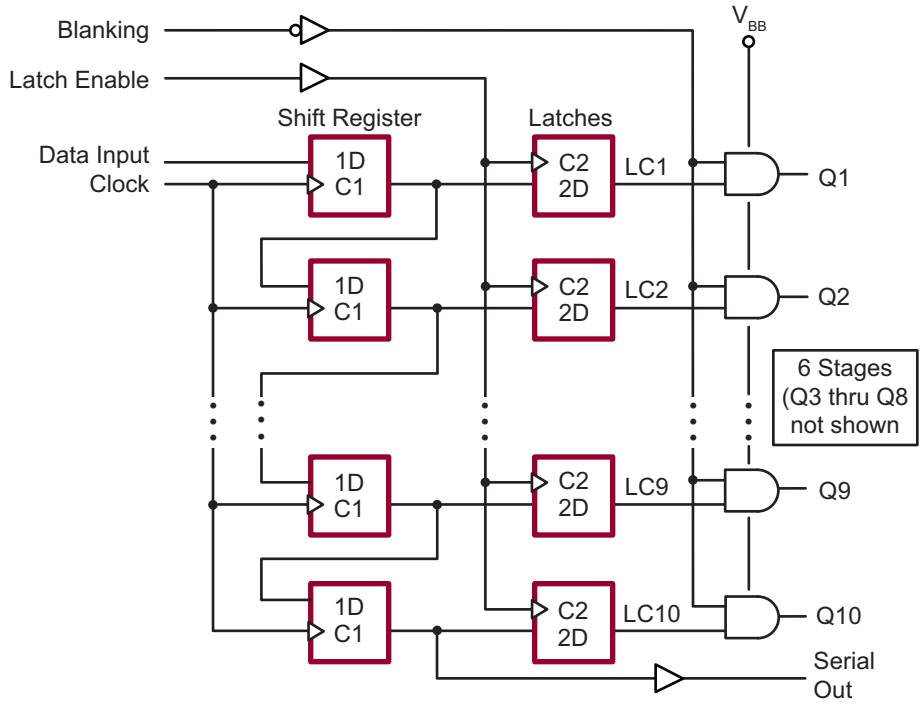
Package Type

20-lead SOW
(Top view)



See Table 2-1 for pin information.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings† (Note 1)

Logic Supply Voltage, V_{DD} (Note 2) 7.5V
Driver Supply Voltage, V_{BB} (Note 2) 90V
Output Voltage (Note 2) 90V
Input Voltage (Note 2) ..... –0.3V to V_{DD} +0.3V
Operating Ambient Temperature, T_A ..... –45°C to +85°C
Continuous Total Power Dissipation at 25°C Free-air Temperature:
20-lead SOW (Note 3) ..... 1500 mW

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Over operating free-air temperature
2: All voltages are referenced to V_{SS}.
3: For operations above 25°C ambient, derate linearly to 85°C at 15 mW/°C.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}	4.5	—	5.5	V	
High Supply Voltage	V_{BB}	20	—	80	V	
Supply Voltage	V_{SS}	—	0	—	V	
High-level Input Voltage (for V_{DD} = 5V)	V_{IH}	3.5	—	5.3	V	
Low-level Input Voltage	V_{IL}	–0.3	—	0.8	V	
Continuous High-level Q Output Current	I_{OH}	25	—	—	mA	
Clock Frequency	f_{CLK}	—	—	5	MHz	
Operating Ambient Temperature	T_A	–40	—	+85	°C	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{DD} = 5V, V_{BB} = 60V, V_{SS} = 0V and T_A = 25°C unless otherwise noted.

Parameter		Sym.	Min.	Typ.	Max	Unit	Conditions
High-level Output Voltage	Q Outputs	V_{OH}	57.5	58	—	V	I_O = +25 mA
	Serial Output		4	4.5	—		V_{DD} = +4.5V, I_{OL} = +100 µA
Low-level Output Voltage	Q Outputs	V_{OL}	—	0.15	1	V	I_O = –100 µA, blanking input at V_{DD}
	Serial Output		—	0.05	0.1		V_{DD} = +4.5V, I_O = –100 µA
Low-level Q Output Current (Pull-down Current)		I_{OL}	60	80	—	µA	T_A = Max, V_{OL} = +0.7V (Note 1)
Off-state Output Current		$I_{O(OFF)}$	—	–1	–15	µA	V_O = 0V, blanking input at V_{DD} (Note 1)
High-level Input Current		I_{IH}	—	—	1	µA	V_{IN} = V_{DD}
Supply Current from V_{DD} (Standby)		I_{DD}	—	10	50	µA	All inputs at 0V, one Q output high
			—	10	50		All inputs at 0V, all Q outputs low

Note 1: All typical values are at T_A = 25°C except for I_{OL} and $I_{O(OFF)}$.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: V_{DD} = 5V, V_{BB} = 60V, V_{SS} = 0V and T_A = 25°C unless otherwise noted.

Parameter	Sym.	Min.	Typ.	Max	Unit	Conditions
Supply Current from V_{BB}	I_{BB}	—	0.05	0.1	mA	All outputs low, all Q outputs open
		—	0.05	0.1		All outputs high, all Q outputs open

Note 1: All typical values are at T_A = 25°C except for I_{OL} and $I_{O(OFF)}$.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Timing requirements are over the recommended operating conditions.

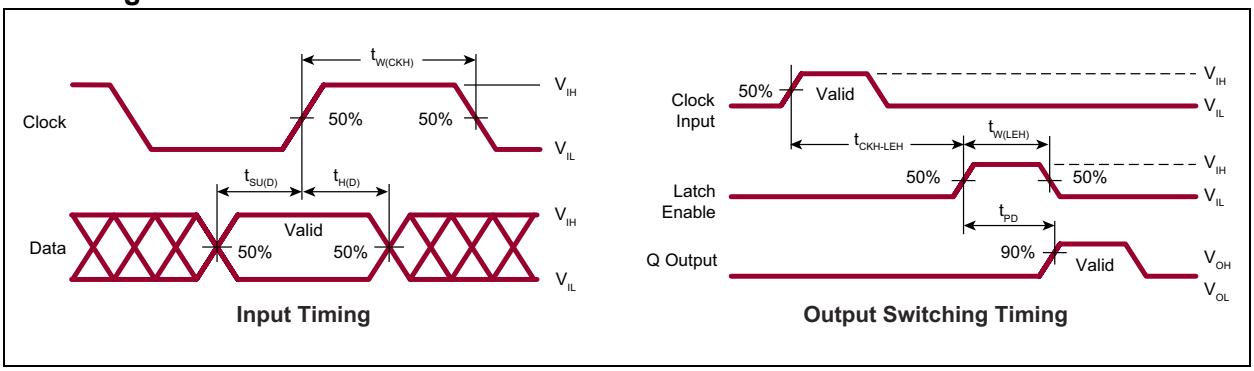
Parameter	Sym.	Min.	Typ.	Max	Unit	Conditions
Pulse Duration, Clock High	$t_{W(CKH)}$	100	—	—	ns	
Pulse Duration, Latch Enable High	$t_{W(LEH)}$	100	—	—	ns	
Setup Time, Data before Clock	$t_{SU(D)}$	50	—	—	ns	
Hold Time, Data after Clock	$t_{H(D)}$	50	—	—	ns	
Delay Time, Clock to Latch Enable High	$t_{CKH-LEH}$	50	—	—	ns	
Propagation Delay Time, Latch Enable to Output	t_{PD}	—	300	—	ns	**Note 1**

Note 1: Switching characteristics, V_{BB} = 60V, T_A = 25°C

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–40	—	+85	°C	
PACKAGE THERMAL RESISTANCE						
20-lead SOW	θ_{JA}	—	66	—	°C/W	

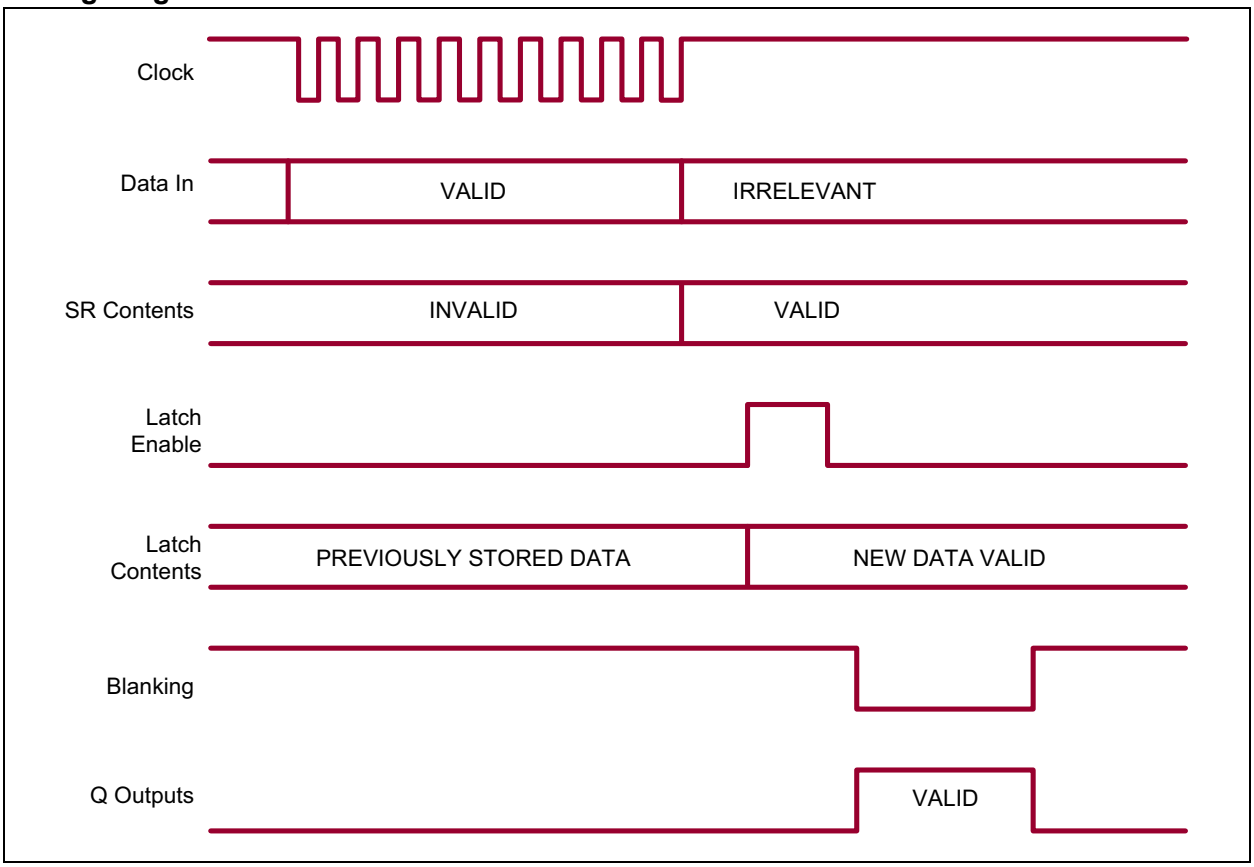
Switching Waveforms



Input Timing

Output Switching Timing

Timing Diagram



2.0 PIN DESCRIPTION

The details on the pins of HV6810 are listed on Table 2-1. Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Q8	High-voltage output
2	Q7	
3	Q6	
4	CLOCK	Input data are shifted into the data shift register on the positive edge of the clock.
5	VSS	Usually V_{SS} = 0V; ground connection
6	N/C	No connection
7	VDD	Low-voltage power supply
8	LE (STROBE)	When LE is high, the shift register output is latched to Q output. When LE stays high, the latches are in Transparent mode.
9	Q5	High-voltage output
10	Q4	
11	Q3	
12	Q2	
13	Q1	
14	BLANKING	When blanking is high, all Q's are forced to a Low state regardless of data in each channel.
15	DATA IN	Input data for the input shift register
16	VBB	High-voltage power supply
17	SERIAL DATA OUT	Output data from the shift register
18	N/C	No connection
19	Q10	High-voltage output
20	Q9	

3.0 FUNCTIONAL DESCRIPTION

Follow the steps below to power up and power down the HV6810.

POWER-UP AND POWER-DOWN SEQUENCE [1]

Power-up		Power-down	
Step	**Description**	**Step**	**Description**
1	Connect ground V_{SS}.	1	Remove V_{BB}.
2	Apply V_{DD}.	2	Remove all inputs.
3	Set all inputs (Data, CLK, Enable, etc.) to a known state.	3	Remove V_{DD}.
4	Apply V_{BB}.	4	Disconnect ground V_{SS}.

Note 1: The V_{BB} should not drop below V_{DD} or float during operation.

FUNCTION TABLE [1]

Serial Data Input	Clock Input	Shift Register Contents				Serial Data Output	LE Strobe Input	Latch Contents				Blanking Input	Output Contents			
		I_1	I_2	I_3... I_{N-1}	I_N			I_1	I_2	I_3... I_{N-1}	I_N		I_1	I_2	I_3... I_{N-1}	I_N
H	L to H	H	R_1	R_2...R_{N-2}	R_{N-1}	R_{N-1}	—	—	—	—	—	—	—	—	—	—
L	L to H	L	R_1	R_2...R_{N-2}	R_{N-1}	R_{N-1}	—	—	—	—	—	—	—	—	—	—
X	H to L	R_1	R_2	R_3...R_{N-1}	R_N	R_N	—	—	—	—	—	—	—	—	—	—
—	—	X	X	X...X	X	X	L	R_1	R_2	R_3...R_{N-1}	R_N	—	—	—	—	—
		P_1	P_2	P_3...P_{N-1}	P_N	P_N	H	P_1	P_2	P_3...P_{N-1}	P_N	L	P_1	P_2	P_3...P_{N-1}	P_N
		—	—	—	—	—	—	X	X	X...X	X	H	L	L	L...L	L

Note 1: L = Low logic level
H = High logic level
X = Don't care
P = Present state
R = Previous state

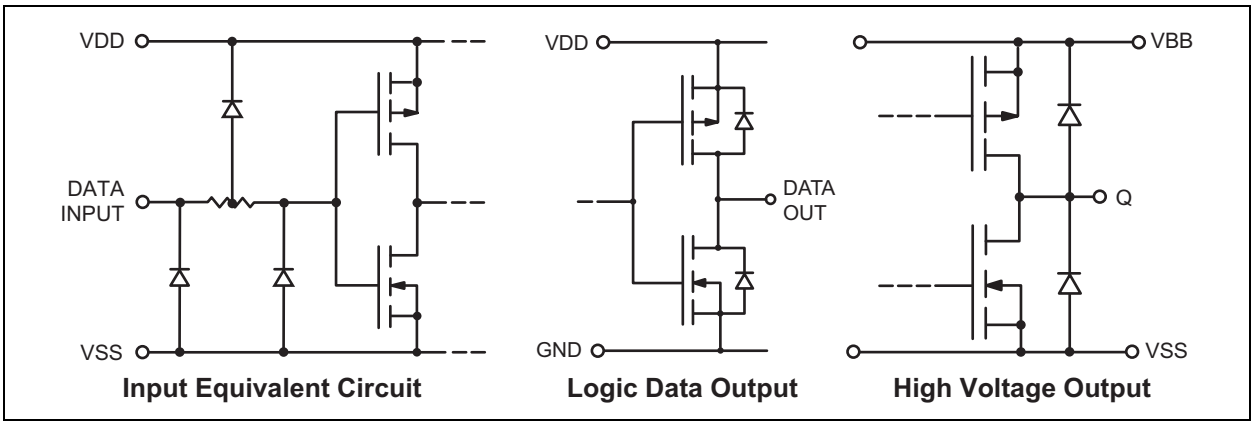
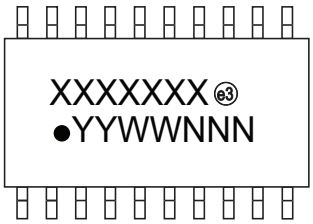


FIGURE 3-1: *Input and Output Equivalent Circuits.*

4.0 PACKAGE MARKING INFORMATION

4.1 Packaging Information

20-lead SOW



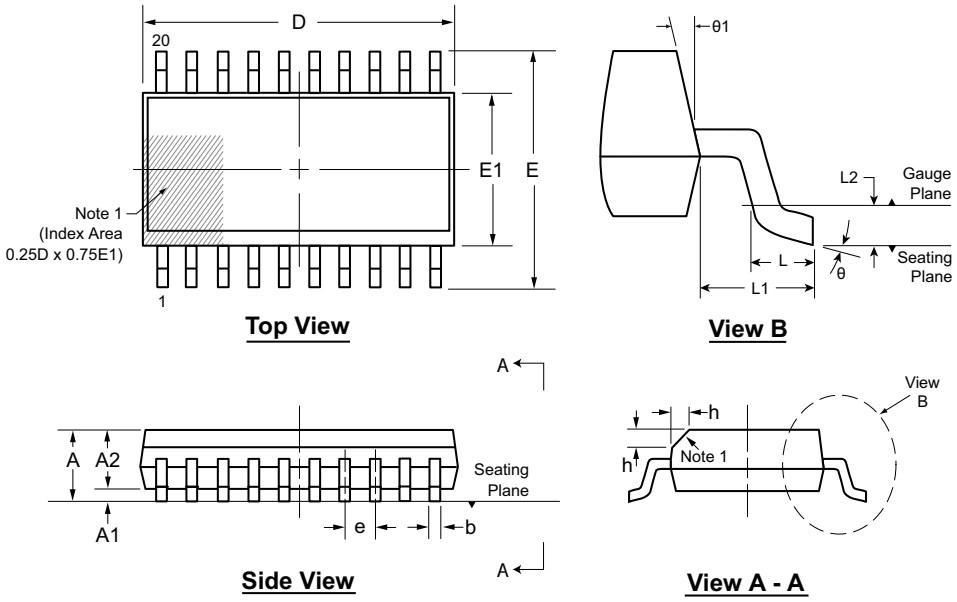
Example

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

20-Lead SOW (Wide Body) Package Outline (WG)

12.80x7.50mm body, 2.65mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.15*	0.10	2.05	0.31	12.60*	9.97*	7.40*	1.27 BSC	0.25	0.40	1.40 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	12.80	10.30	7.50		-	-			-	-
	MAX	2.65	0.30	2.55*	0.51	13.00*	10.63*	7.60*		0.75	1.27			8°	15°

JEDEC Registration MS-013, Variation AC, Issue E, Sep. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2016)

- Converted Supertex Doc# DSFP-HV6810 to Microchip DS20005626A
- Removed the PJ package option
- Changed the quantity of the WG package from 1000/Reel to 1600/Reel
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV6810	=	10-Channel Serial-Input Latched Display Driver
Package:	WG	=	20-lead SOIC
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	1600/Reel for a WG Package

Example:

a) HV6810WG-G: 10-Channel Serial-Input Latched Display Driver, 20-lead SOIC, 1600/Reel for a WG Package

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